USB3.0 Video Capture Board

[SVI-09]

Hardware Specification

Rev.1.0

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	2019/1/9	New File (Equivalent to Japanese version 2.1)	S.Usuba

Index

1. Outline

This document is a hardware specification of the board "SVI-09" for capturing video signals output from the image sensor with USB 3.0 connection.

SVI-09 has SVI compatible mode. The SVI compatible mode is for users who are using our product SVI series in the past and you can use the software for SVI-07 of the previous product as it is.

SVI-09 supports uncompressed video transfer of 1920 x 1080 60 FPS or more.

1.1. Specifications

- Power : USB Bus Supply (External Power Input Applicable) / +5V 0.7A typ.
- Input format (via CN3, 4):
  - Parallel video signal (PCLK/VSYNC/HSYNC; Embedded Sync (BT.656))
    - SVI-09 is compatible with sensors with PCLK 100 MHz or less
    - Input Bit Width: 8bit / 16bit / 24bit / 32bit
- Input format (via CN5):
  - Parallel video signal (PCLK/VSYNC/HSYNC; Embedded Sync (BT.656))
    - PCLK –
    - Input Bit Width:: –
  - LVDS Signal (max. 12 Data Lanes + 2 Clock Lanes)
- Input resolution: max. 8191x8191 pix,
- Output: USB3.0 (vender driver)
- FPGA: XC7A35T-1FGG484C

2. SVI compatible mode operation details

This chapter describes the SVI compatible mode.

2.1. Main Functions and Features of SVI compatible mode

- It is a mode compatible with our conventional SV series products.
- It operates using the API provided by our company and a driver.
- It does not correspond to SVI-06Q, SVI-07 board.
- SVI-09 can capture video at twice the speed of SVI-06.(1080p 30fps → 60fps)

2.2. Connection Example

2.3. Procedure for setting in SVI compatibility mode

The necessary setting items are listed below.

・Setting of target side power supply voltage (VDDL)

Before connecting the target device, it is necessary to adjust VDDL to the IO voltage of the image sensor or conversion board. The default is set to 3.3V.

VDDH can also be used as usual. The default is set to 3.3V.

・The initial value of the master clock to the target is 54 MHz. Unlike SVI-06, there is no clock generator on the board, so it can change the setting from the PC application after startup.

・DIP SW setting

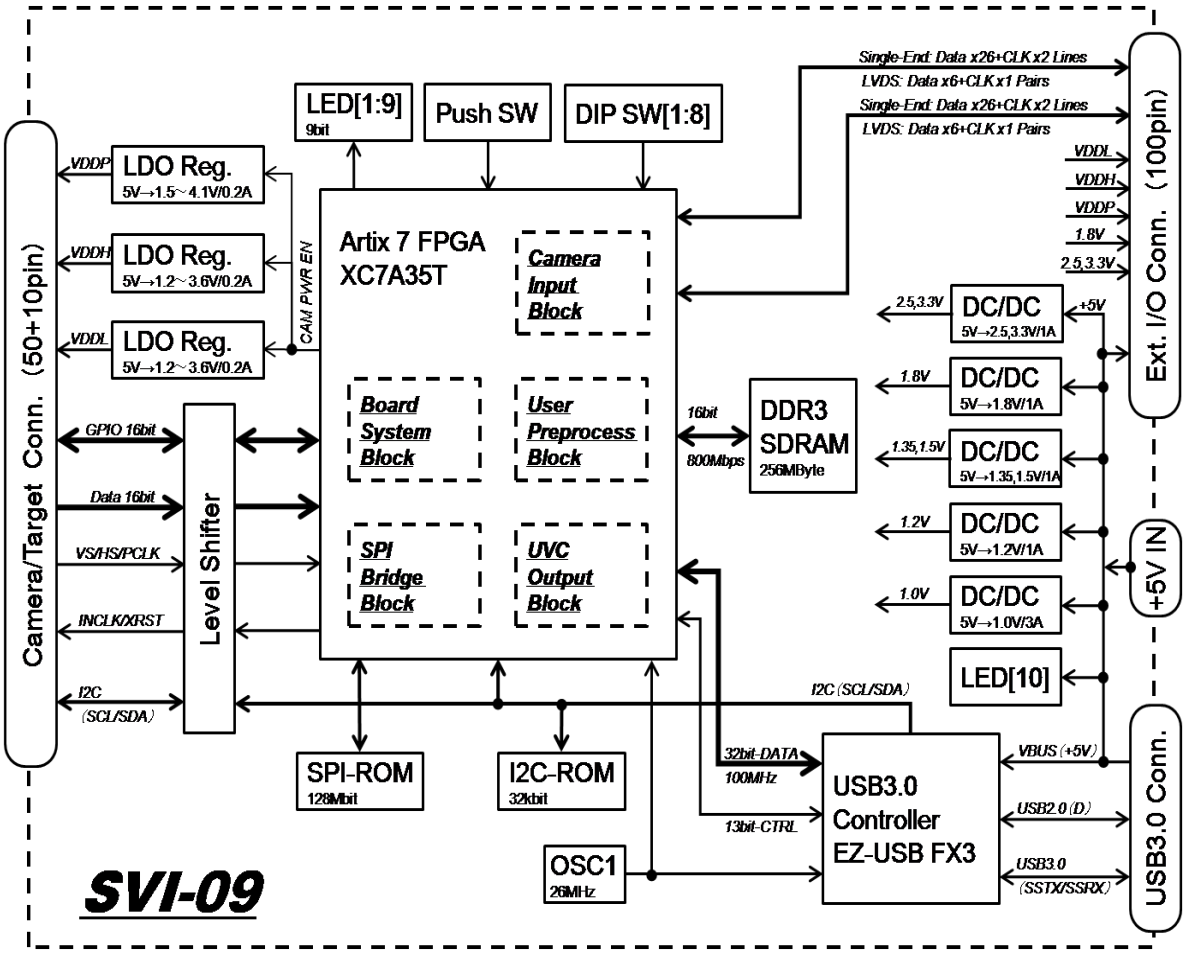
It is necessary to set the DIP SW, such as dividing the master clock output to the target device, setting the camera power OFF at the time of activation, specifying the board number. For the setting, see section 6.2.

・Initial setting from PC

It is necessary to perform initial setting such as pixel format from our application or an application using our API.
The initial setting is done by the software "SVImon" included in the CD. For the operation of SVImon, refer to "SVI Software Manual".

3. Block Diagram of SVI-09

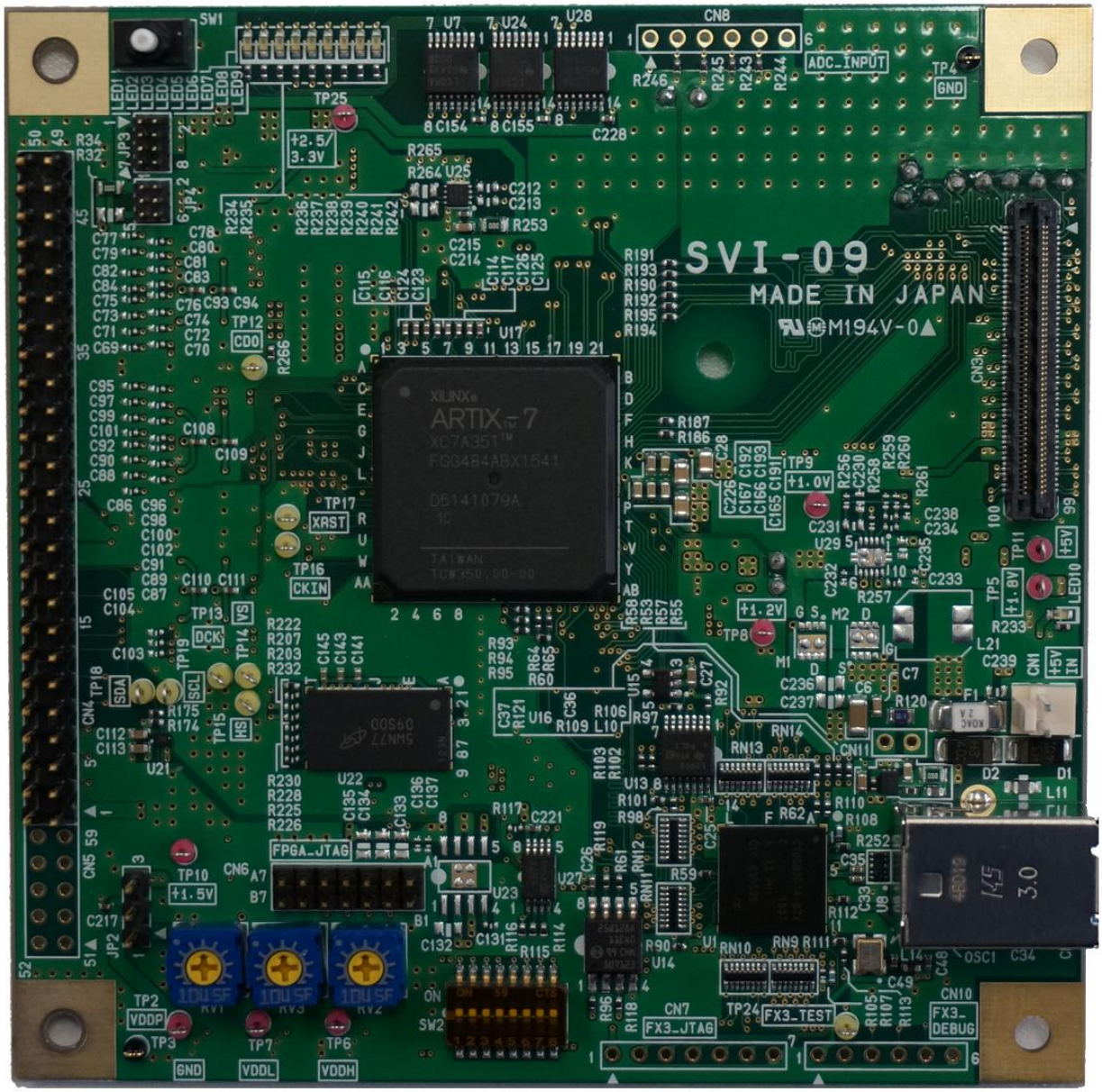
The schematic block diagram of the SVI-09 board is shown below.



4. Exterior of SVI-09 Board

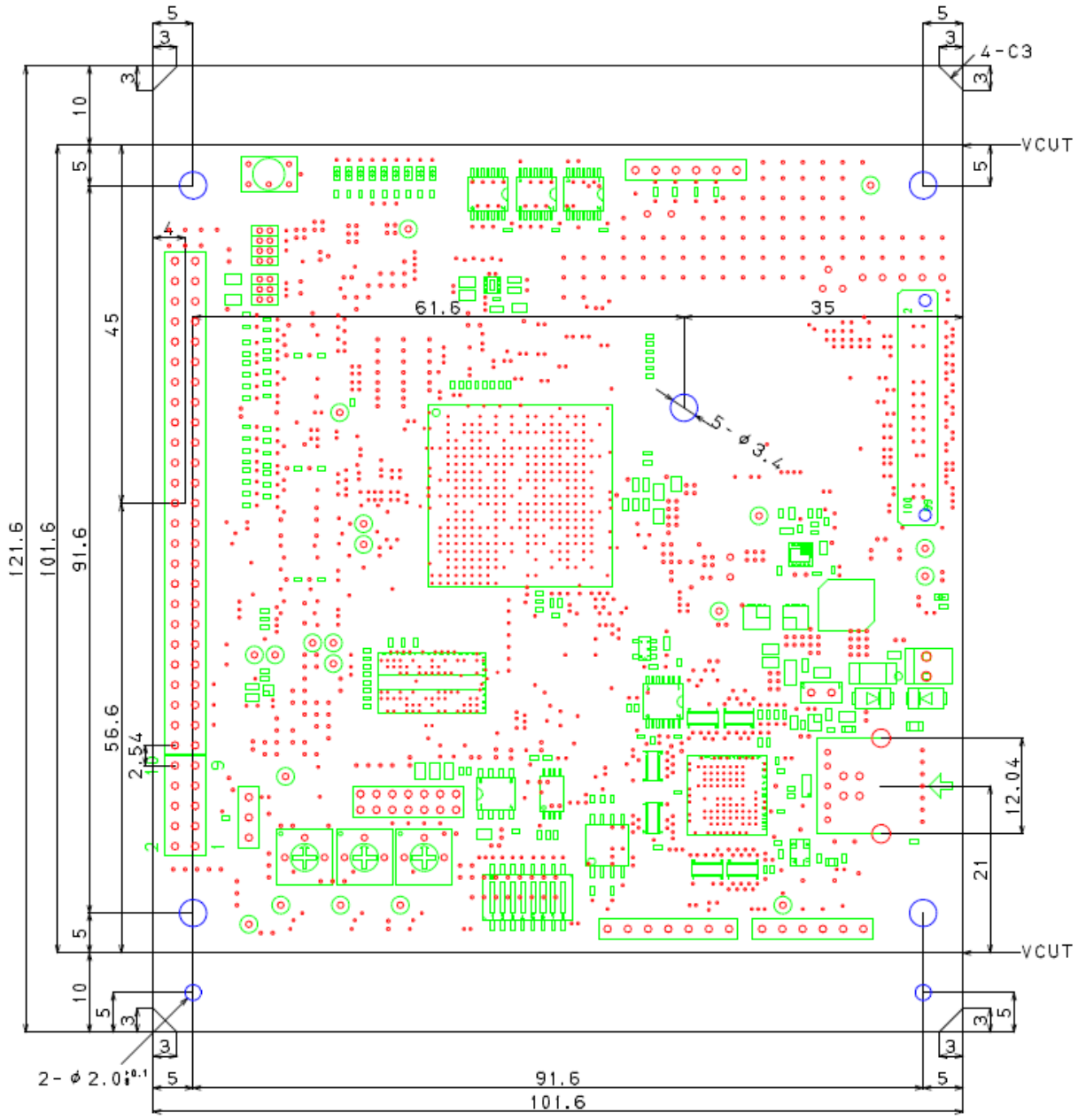
Below are photos and diagrams on the outline of the SVI – 09 board.

4.1. Exterior Photos



4.2. Dimensional drawing

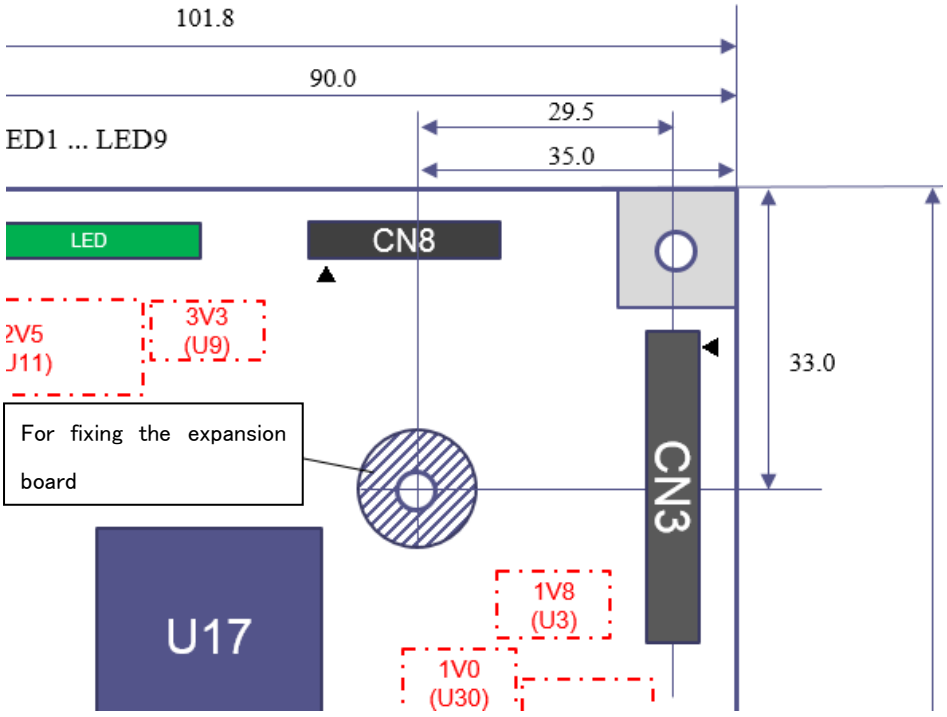
Below is the dimension drawing of SVI-09 board. It is 101.6 [mm] as well as the conventional SVM-03 board both vertically and horizontally, and it is smaller than the SVI-06/07 board.



4.2.1. CN3 position relation

The positional relationship between CN3 and expansion board fixing hole is shown below.

CN3 center and the expansion board fixing hole are on the same line, but please note that it is not on the same line as the hole position at the 4 corners of the board.



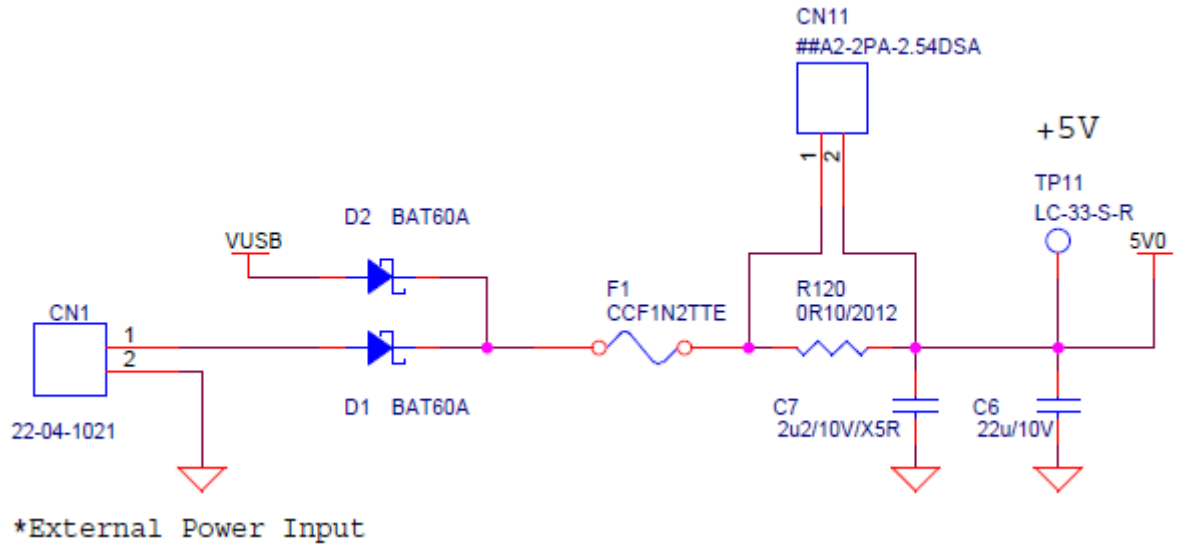
5. Connector specification

This chapter describes the specifications of connectors that should be considered when connecting to a camera or during normal use. Other connectors are described in the Appendix.

5.1. CN1 : Sub power supply connector

It is a power connector for use when power is not supplied via USB bus power or when USB bus power can not meet the power capacity.

Connector		22-04-1021: Molex					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	+5V	IN	DC5V Input	2	GND	-	GND



- CN1 and + 5V from the USB connector are connected by diode OR as shown in the above circuit diagram.

5.2. CN3: Target Connector A

It is a connector for connecting the target image sensor. For signals exceeding the support range of CN 4, 5 such as LVDS signal, you need to use this connector.

- The following pin assignments are for reference only. Detailed functions of pins will be determined according to the system.

Connector		LSHM-150-03.0-F-DV-A-N-K-TR / Samtec	
Pin#	Name	Alternate function (reference)	Description
1	EXCLK1	INCK_1 / INCK	EXCLK [1:0]: Clock Input / Output
2	EXCLK0	INCK_2 / XCLR	
3	EXBUS1	XCLR_1 / VS	EXBUS [17:0]: GPIO
4	EXBUS0	XCLR_2 / HS	
5	EXBUS3	I2CSCL_1 / SPISCK	
6	EXBUS2	I2CSCL_2 / SPIXCE	
7	EXBUS5	I2CSDA_1 / SPISDO	
8	EXBUS4	I2CSDA_2 / SPISDI	
9	GND		
10	GND		
11	EXADC_N1	EXTVS_C	EXADC_N [3:0]: ADC Input - / GPIO
12	EXADC_N0	EXTHS_C	
13	EXADC_P1	PINSWAP_1	EXADC_P [3:0]: ADC Input + / GPIO
14	EXADC_P0	PINSWAP_2	
15	EXADC_N3	GPIO-1_1	
16	EXADC_N2	GPIO-1_2	
17	EXADC_P3	BTA_1	
18	EXADC_P2	BTA_2	
19	GND		
20	GND		
21	EXBUS7	LP-A-N_1	LP-x-N_n: MIPI Low Power (LVCMOS) - (n determines channel number (0-1))
22	EXBUS6	LP-A-N_2	
23	EXBUS9	LP-A-P_1	LP-x-P_n: MIPI Low Power (LVCMOS) +
24	EXBUS8	LP-A-P_2	
25	EXBUS11	LP-B-N_1	
26	EXBUS10	LP-B-N_2	
27	EXBUS13	LP-B-P_1	
28	EXBUS12	LP-B-P_2	
29	EXBUS15	LP-C-N_1	
30	EXBUS14	LP-C-N_2	
31	EXBUS17	LP-C-P_1	
32	EXBUS16	LP-C-P_2	
33	EXLVDS_N1	LP-D-N_1	
34	EXLVDS_N0	LP-D-N_2	
35	EXLVDS_P1	LP-D-P_1	
36	EXLVDS_P0	LP-D-P_2	
37	GND		
38	GND		

Connector		LSHM-150-03.0-F-DV-A-N-K-TR / Samtec	
Pin#	Name	Alternate function (reference)	Description
39	EXLVDS_N3	HS-A-N_1	EXLVDS_N [11:0]: LVDS - (configurable as GPIO) HS-x-N_n: MIPI High Speed (LVDS) -
40	EXLVDS_N2	HS-A-N_2	
41	EXLVDS_P3	HS-A-P_1	EXLVDS_P [11:0]: LVDS + (configurable as GPIO) HS-x-P_n: MIPI High Speed (LVDS) +
42	EXLVDS_P2	HS-A-P_2	
43	GND		
44	GND		
45	EXLVDS_N5	HS-B-N_1	
46	EXLVDS_N4	HS-B-N_2	
47	EXLVDS_P5	HS-B-P_1	
48	EXLVDS_P4	HS-B-P_2	
49	GND		
50	GND		
51	EXLVDS_CLK_N1	HS-E-N_1	EXLVDS_CLK_N [1:0]: LVDS Clock - / GPIO
52	EXLVDS_CLK_N0	HS-E-N_2	
53	EXLVDS_CLK_P1	HS-E-P_1	EXLVDS_CLK_P [1:0]: LVDS Clock - / GPIO
54	EXLVDS_CLK_P0	HS-E-P_2	
55	GND		
56	GND		
57	EXLVDS_N7	HS-C-N_1	
58	EXLVDS_N6	HS-C-N_2	
59	EXLVDS_P7	HS-C-P_1	
60	EXLVDS_P6	HS-C-P_2	
61	GND		
62	GND		
63	EXLVDS_N9	HS-D-N_1	
64	EXLVDS_N8	HS-D-N_2	
65	EXLVDS_P9	HS-D-P_1	
66	EXLVDS_P8	HS-D-P_2	
67	GND		
68	GND		
69	EXLVDS_N11	LP-E-N_1	
70	EXLVDS_N10	LP-E-N_2	
71	EXLVDS_P11	LP-E-P_1	
72	EXLVDS_P10	LP-E-P_2	
73	VDDL		VDDL Power Output
74	VDDH		VDDH Power Output
75	VDDL		
76	VDDH		
77	5V0		Connected to +5V
78	VDDP		VDDP Power Output
79	5V0		
80	VDDP		

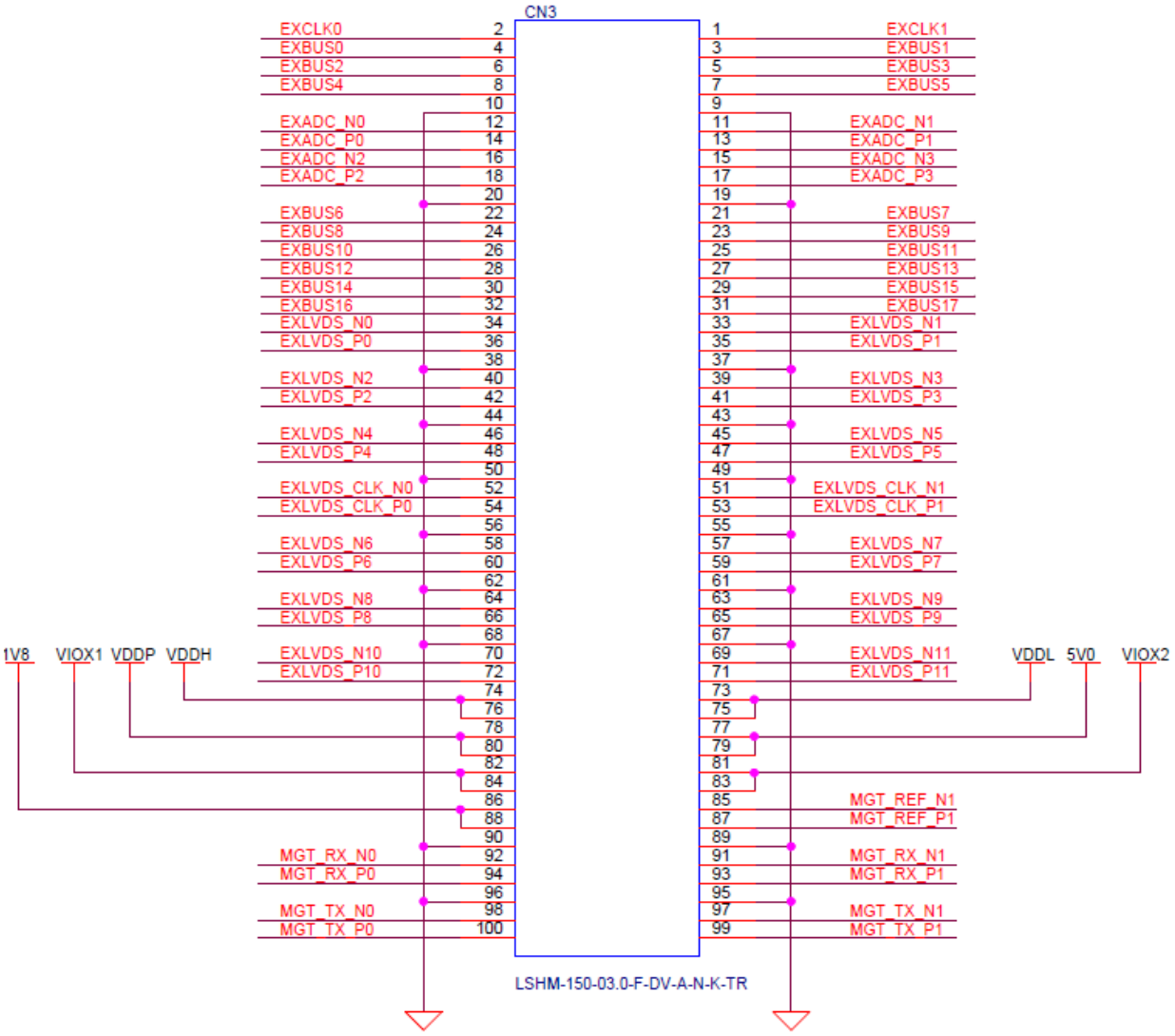
Connector		LSHM-150-03.0-F-DV-A-N-K-TR / Samtec	
Pin#	Name	Alternate function (reference)	Description
81	VIOX2		IO Level Voltage 2
82	VIOX1		IO Level Voltage 1
83	VIOX2		
84	VIOX1		
85	MGT_REF_N1		MGT Referential Input -
86	1V8		Connected to +1.8V
87	MGT_REF_P1		MGT Referential Input +
88	1V8		
89	GND		
90	GND		
91	MGT_RX_N1		MGT Input 1-
92	MGT_RX_N0		MGT Input 0-
93	MGT_RX_P1		MGT Input 1+
94	MGT_RX_P0		MGT Input 0+
95	GND		
96	GND		
97	MGT_TX_N1		MGT Output 1-
98	MGT_TX_N0		MGT Output 0-
99	MGT_TX_P1		MGT Output 1+
100	MGT_TX_P0		MGT Output 0+

- About Single-ended IO Voltage Level

When used as a single-ended IO pin, two types of voltage levels can be used with pins. The correspondence is as follows.

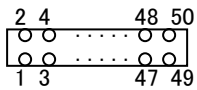
EXCLK[1:0], EXBUS[5:0], EXADC_xx: VDDX1 level

EXBUS[17:6], EXLVDS_xx: VDDX2 level



5.3. **CN4**: Target Connector B

Top View



It is a connector for connecting the target image sensor.

When inputting by parallel connection, input a signal from CN 4 (CN 5 is also used if it exceeds 16 bits).

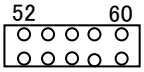
Connector		A1-50PA-2.54DSA: HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	VDDL	OUT	Target IO Power Supply (1.6 – 4.2V adjustable)	2	GND	–	–
3	P0	IN	Input Port 0 / Pixel DATA 16	4	GND	–	–
5	P1	IN	Input Port 1 / DE Input (8-16bit) / Pixel DATA17	6	GND	–	–

7	P2	IN	Input Port 2 / Pixel DATA 18	8	GND	–	–
9	P3	OUT / IN	Output Port 0 / Pixel DATA 24	10	GND	–	–
11	P4	OUT / IN	Output Port 1 / Pixel DATA 25	12	HSYNC	IN	Horizontal Sync Input
13	VSYNC	IN	Vertical Sync Input	14	XRST	OUT	Reset Output
15	VDDH	OUT	Target Power Supply (1.6 – 4.2V adjustable)	16	GND	–	–
17	SDA	IO	I2C_DATA	18	GND	–	–
19	SCL	IO	I2C_CLK	20	GND	–	–
21	DCK	IN	Pixel_CLK (Pixel Clock Input)	22	GND	–	–
23	Y0	IN	Pixel_DATA0	24	GND	–	–
25	Y1	IN	Pixel_DATA1	26	GND	–	–
27	Y2	IN	Pixel_DATA2	28	GND	–	–
29	Y3	IN	Pixel_DATA3	30	GND	–	–
31	Y4	IN	Pixel_DATA4	32	GND	–	–
33	Y5	IN	Pixel_DATA5	34	GND	–	–
35	Y6	IN	Pixel_DATA6	36	GND	–	–
37	Y7	IN	Pixel_DATA7	38	GND	–	–
39	CLKOUT	OUT	Target Ext. Clock Output	40	GND	–	–
41	Y8	IN	Pixel_DATA8	42	Y9	IN	Pixel_DATA9
43	Y10	IN	Pixel_DATA10	44	Y11	IN	Pixel_DATA11
45	Y12	IN	Pixel_DATA12	46	Y13	IN	Pixel_DATA13
47	Y14	IN	Pixel_DATA14	48	Y15	IN	Pixel_DATA15
49	+3.3V	OUT	+3.3V Output (up to 0.3A)	50	P5	OUT / IN	Output Port 2 / Pixel DATA 26

5.4. **CN5**: Target Connector C

It is a connector for connecting the target image sensor.

Top View

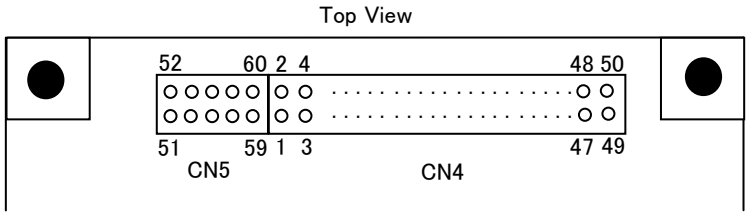


Connector		A1-10PA-2.54DSA: HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
51	P6	OUT/ IN	Output Port 3 / Pixel DATA 27	52	P7	OUT / IN	Output Port 4 / Pixel DATA 28

53	P8	OUT / IN	Output Port 5/ Pixel DATA 29	54	P9	OUT / IN	Output Port 6/ Pixel DATA 30
55	P10	OUT / IN	Output Port 7/ Pixel DATA 31	56	P11	IN	Input Port 3/ Pixel DATA 19
57	P12	IN	Input Port 4/ Pixel DATA 20	58	P13	IN	Input Port 5/ Pixel DATA 21
59	P14	IN	Input Port 6/ Pixel DATA 22	60	P15	IN	Input Port 7/ Pixel DATA 23

- CN5 is optional; in standard SVI-09 this connector is not implemented.
- The input / output direction of Pixel_DATA [31: 24] is changed according to the input bit width setting.

5.5. Relationships between **CN4 and CN5**



- Together with CN5 and CN4, these connectors can be used as a 60P pin header.
- The 60-pin connection connector becomes "Hirose Electric: HIF3BA-60D-2.54R"when connected by cable.
- The 60-pin connection connector becomes "Hirose Electric: HIF3H-60DA-2.54DSA(71)" when connected by board-to-board connect.

5.6. Input Data Format

When YUV or RGB24 format image sensor is connected to SVI-09 board, please connect with the following list.

Format	YUV4:2:2			RGB24
Bit Width	8bit (UYVY/YUY2)	16bit (UYVY)	32bit (UYVY)	24bit
Pixel_DATA [31:24]	-	-	V	-
Pixel_DATA [23:16]	-	-	Y	R
Pixel_DATA [15:8]	-	U, V	U	B
Pixel_DATA [7:0]	Y, U, V	Y	Y	G

- Enable/disable polarity and DE input of VS, HS, DCK can be set arbitrarily.
- DE input is non-compliant with 24bit/32bit input.

6. Details of each part

6.1. **SW1:** Push Switch

It is not normally used.

6.2. **SW2:** DIP Switch

This is a 8-bit switch for setting the various modes of operation of SVI-09.

The following setting is possible by switch SW2.

○ SVI compatible mode

Number #	Name	Turns OFF	Turns ON
1	I2C transfer rate	1 OFF 2 OFF 400Kbps ※default	
2		1 ON 2 OFF 100Kbps	
		1 OFF 2 ON 200Kbps	
		1 ON 2 ON 100Kbps	
3	Board number	3 OFF 4 OFF 0 ※default	
4		3 ON 4 OFF 1	
		3 OFF 4 ON 2	
		3 ON 4 ON 3	
5	Master clock division	1/1	1/2 ※default
6	Camera power setting	Power on at startup ※default	Power off at startup
7	Operation mode setting	SVI compatible ※default	Update Mode
8	Reserved	OFF	

6.3. **LED1-9**: Working State Indicator

This LED displays the operating status of the board or FPGA.

○ SVI compatible mode

LED#	Description
1	Lights up when power is being supplied to Target.
2	Lights up when the clock supplied to Target is locked.
3	Lights up when a video sync signal is detected from Target.
4	This LED is switched ON/OFF in the V-sync synchronization signal from the target at a cycle of three-minute laps. When input video signal is 30 FPS, this LED blinks 5 times in 1 second.
5	Lights up when the Data Capture Block is idle.
6	Lights when the destination FITB of the Data Capture Block is Secondary, and goes dark when it is Primary.
7	Lights up when Primary-FITB is Frame write Ready.
8	Lights up when Frame Uploader Block is transferring Frame.
9	Lights up when Read / IN transfer of FX3-I / F Block is Done.

6.4. **RV1, RV2, RV3**: VDDH, VDDL, VDDP adjustment variable resistor

These are variable resistors to adjust voltage level or power supply on the SVI-09 board for the target device. VDDL, VDDH can be adjusted from 1.2V～3.6V. VDDP can be adjusted from 1.5V – 4.1V.

Since VDDL is connected to voltage translator ICs, this voltage level must be equal to the parallel input signal level and GPIO voltage level. On the other hand, VDDH and VDDP are just connected to the target connector and this is not used inside the board. Both voltages can be used as the power supply of external target device. For detail of VDDL、VDDH, VDDP please refer section 8.

In default, VDDL, VDDH, and VDDP are set to 3.3 V. It is necessary to adjust according to the voltage of the target side before use.

6.5. **JP2:** Jumper for VDDP selection

The VDDP power output of the SVI-09 board is selected by JP2 from two systems of + 5V output from USB power supply and variable power supply from on – board regulator.

JP2	VDDP
1-2 short circuit	variable power supply
2-3 short circuit	VUSB (+5V)

6.6. **JP3, JP4:** Jumpers for setting VIOX1, VIOX2

On the SVI-09 board, a connector CN 3 is newly added in addition to the IO connector mounted on the conventional board. For single-ended IO of CN3, two IO voltages can be set, and this IO voltage (VIOX1, VIOX2) is set by JP3, JP4. The voltage setting values are as shown in the table below. **Please be aware that turning on the power of the SVI-09 board without inserting the jumper pins of JP3 and JP4 will cause a malfunction.**

For the correspondence between VIOX1, VIOX2 and each IO pin of CN3, refer to the pin assignment chart.

JP3 voltage setting (VIOX1)

JP3	VIOX1
1-2 short circuit	1.8V
3-4 short circuit	2.5V
5-6 short circuit	3.3V

JP4 voltage setting (VIOX2)

JP4	VIOX2
1-2 short circuit	1.8V
3-4 short circuit	2.5V
5-6 short circuit	3.3V

7. Check Terminal

7.1. **TP2:** VDDH check terminal (red)

This is the check terminal used to adjust the VDDH.

7.2. **TP4:** VDDL check terminal (red)

This is the check terminal used to adjust the VDDL.

7.3. **TP1, 3, 5, 6:** Voltage check terminal (red)

This is check terminal for each supply voltage required by the SVI-09 board operation. In normal use, there is no need to check. Also, please stop extract the power from this check terminal to supply power to external modules.

7.4. **TP7-10:** GND check terminal (black)

Please use it as a GND terminal at the time of VDDH and VDDL adjustment.

7.5. **TP11-33:** Signal check terminal (yellow)

This is the check terminal of the target signal. The silk of each signal is stamped. Use it to connect the measuring instrument.

8. Target Power Supply

In addition to the power supply of the IC mounted in the board, the SVI-09 has multiple variable voltage power supplies for the target device.

8.1. **VDDH**: System Power Supply for Target Device

VDDH is system power supply of image sensor or target device. VDDH is just connected to the target connector and this is not used inside the board. This is adjusted by volume RV1 on the SVI-09 board from 1.6V to 4.2V. Output current rating is 200mA.

In default, it is set to +3.3V.

8.2. **VDDL**: IO Power Supply for Target Device

VDDL is IO power supply of image sensor or target device. This is adjusted by volume RV2 on the SVI-09 board from 1.6V to 4.2V. Output current rating is 200mA.

The SVI-09 is equipped with a level converter IC, and when using CN 4, 5, IO signals are converted from VDDL level to internal IO level. Thus, **even if VDDL is not used in the target device, VDDL voltage level must be adjusted to the output IO voltage level of the target.**

When CN3 is used, the IO voltage (VIOX1, VIOX2) of CN3 is selected independently of the voltage of VDDL because it is selected by jumper JP3, 4.

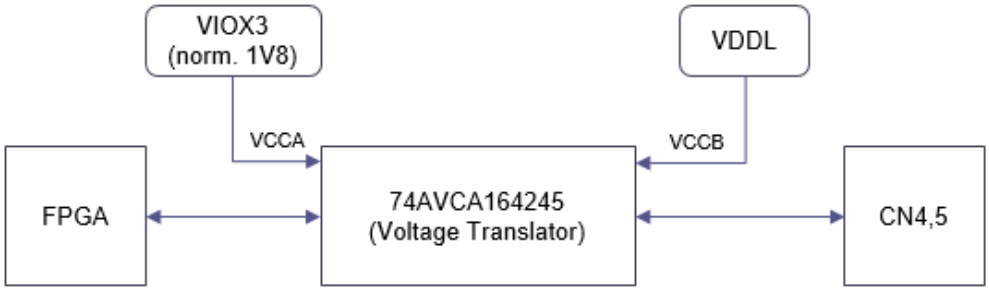
In default, it is set to +3.3V.

8.3. **VDDP**: Auxiliary Power Supply for Target Device

VDDP is assumed to be used as an auxiliary power source for image sensors and target devices. When the state of jumper JP2 is short-circuited between 2 and 3, VDDP can be adjusted with the variable resistor RV3 mounted on the board. It can be adjusted in the range of about 1.6 V to 4.2 V, and it can output current of about 200 mA. When JP2 is short-circuited between 1 and 2, + 5V of USB power supply is output directly to VDDP.

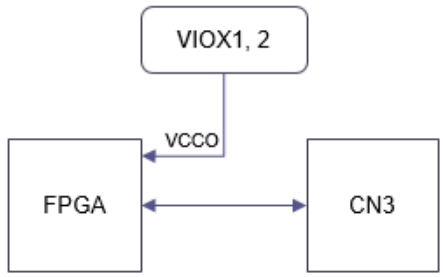
In default, it is set to +3.3V.

8.4. CN4,5 IO Schematic Diagram



- The IO voltage of each pin is determined by the voltage of VDDL.

8.5. CN3 IO Schematic Diagram



- The IO voltage of each pin is determined by the voltage of VIOX1, VIOX2.

9. Notes

For proper use of this board, be sure to follow the following precautions.

1. To update the farm and FPGA, use dedicated control software from the host PC.
2. When connecting and disconnecting targets, be sure to turn off the power supply of the SVI-09 board.
3. For power supply to this board, please use a power supply with sufficient margin of current capacity. Please power supply from the PC under your own risk. In the unlikely event that the PC has been damaged, we can not assume any responsibility.
4. The contents of this document may be changed in the future without notice.
5. Reprinting of part or the whole of the contents of this document is strictly forbidden.
6. Through extreme care has been taken in preparing this document, if you find any ambiguous points or errors, or if you would like to make any comments on the document itself or its content, please contact to sv-support@net-vision.co.jp

10. Appendix

10.1. CN2: USB3.0 Connector

USB 3.0 connector to connect to the host PC. A commercially available USB 3.0 cable is available. This connector is used for power supply of SVI-09.

Connector		USB30B-09K-PC: JC Electronics Corporation					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	VBUS	IN	+ 5v Bus Power	2	D-	I/O	USB 2.0 Differential Pair-
3	D+	I/O	USB 2.0 Differential Pair+	4	GND	-	GND (Power)
5	SSRX-	IN	USB 3.0 receiver Differential pair -	6	SSRX+	IN	USB 3.0 receiver Differential pair +
7	GND DRAIN	-	GND (Signal)	8	SSTX-	OUT	USB 3.0 Transmission Differential pair -
9	SSTX+	OUT	USB 3.0 Transmission Differential pair +				

10.2. CN6: FPGA-JTAG Connector

The JTAG port used to write to the SPI-ROM of the FPGA bit stream or to debug a running FPGA. You do not need to use it in normal operation.

-The direction is seen from the FPGA.

Connector		A3B-14PA-2DSA(71): HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	GND	-		2	VREF	OUT	Reference Voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	Disconnected
13	GND	-		14	NC	-	Disconnected

- **We do not guarantee the operation when you use it.**

10.3. **CN7:** FX3-JTAG Connector

The JTAG port used to debug the FX3 firmware. You do not need to use it in normal operation.

-The direction is seen from the FX3.

Connector		A2-7PA-2.54DSA(71): HRS					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	+3.3V	OUT	Reference Voltage (3.3V)	2	TMS	IN	JTAG-TMS
3	TCK	IN	JTAG-TCK	4	TDO	OUT	JTAG-TDO
5	TDI	IN	JTAG-TDI	6	TRST	OUT	Reset
7	GND	-					

- CN7 is optional. The PIN header is not implemented.
- **We do not guarantee the operation when you use it.**