

GVO-4963 / NV025-A
(GVIF2 Serializer Board)
Hardware Specification

Rev.1.0

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	11. Dec., 2024	New File (Translation of Japanese edition ver.2.1)	R. Sugo

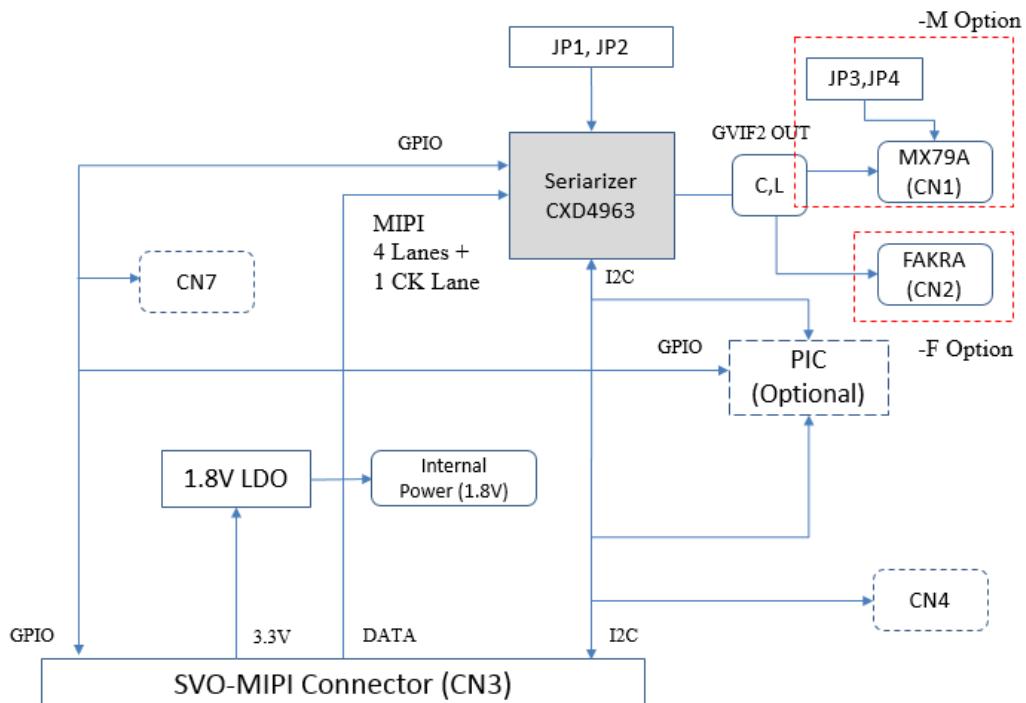
Index

1.	Overview	2
2.	Drawing	4
2.1	Connector Layout Diagram	4
2.2	Shape of The Board.....	5
3.	Details	6
3.1	Connectors List	6
3.2	Connectors Details	6
3.3	Switch	9
3.4	Jumper Settings	9
3.5	LED Indicator.....	10
3.6	Power Supply.....	10
3.7	GPIO	10
3.8	MIPI Signal Input Assignment.....	10
4.	Specifications	11
5.	Appendix	12
5.1	Figure of Board Dimensions.....	12
5.2	PIC Microcontroller Peripheral Circuit Diagram.....	13

1. Overview

This is a hardware specification of GVO-4963 / NV025-A (GVIF2 Serializer board). This board is mounted the SONY serializer CXD4963 and is used to convert MIPI video signals to GVIF2 signals. This board has a GVIF2 output connector and a MIPI input connector that can be connected to our SV board. It can be used to emulate GVIF2 cameras.

Block Diagram

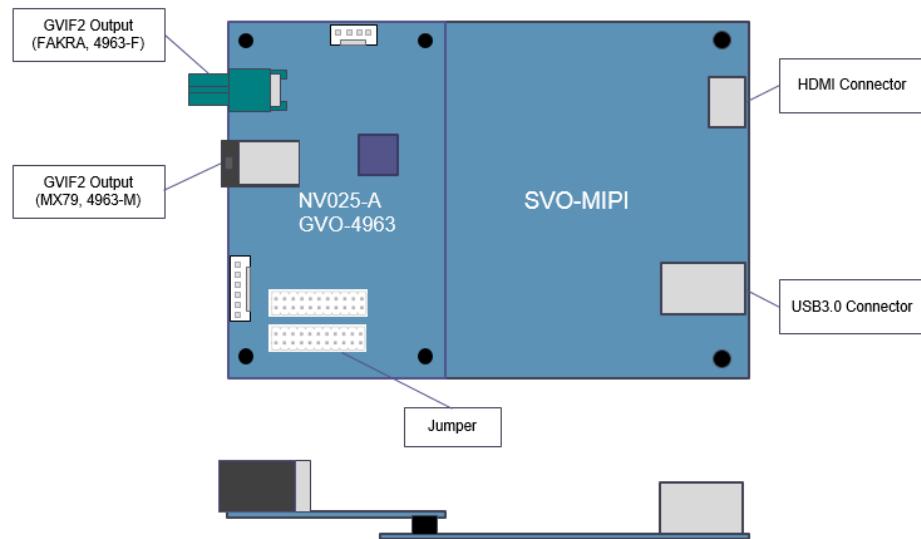


For the GVO-4963-M specification, the GVIF2 output is connected to the JAE MX79A connector. In this case, the FAKRA connector is unmounted and cannot be used. For the GVO-4963-F specification, the GVIF2 output is connected to the FAKRA connector. In this case, the MX79A connector cannot be used.

The MIPI signal input connector (CN3) is intended to be connected to our video output SV board and can be directly connected to it. The board power is supplied from the SV board via connector CN3. It does not support external power supply. As an option, this GVO-4963 board has a pattern that allows a PIC microcontroller to be mounted for I2C slave emulation.

The figure below shows a connection image of GVO-4963 and the SV board. Since the screw hole positions are the same for both boards, it is possible to fix the boards with spacers.

Board Connection Image

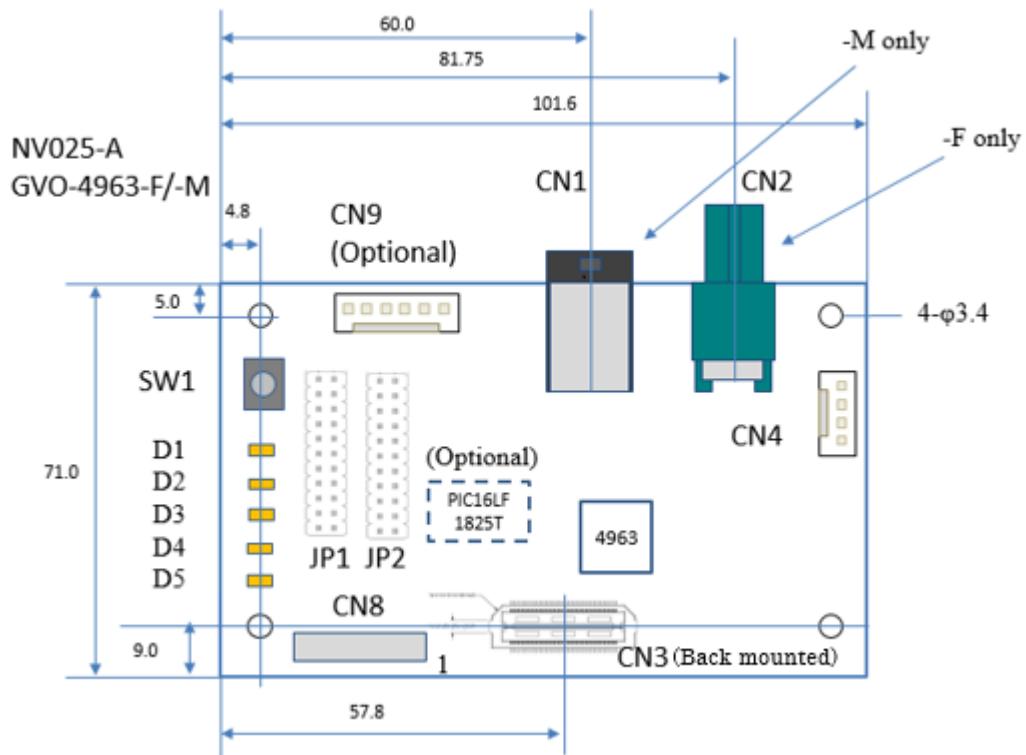


2. Drawing

2.1 Connector Layout Diagram

The figure below shows the arrangement of the main connectors on the GVO-4963 board. Pin numbers and pin assignments are shown in “Connectors Details” section.

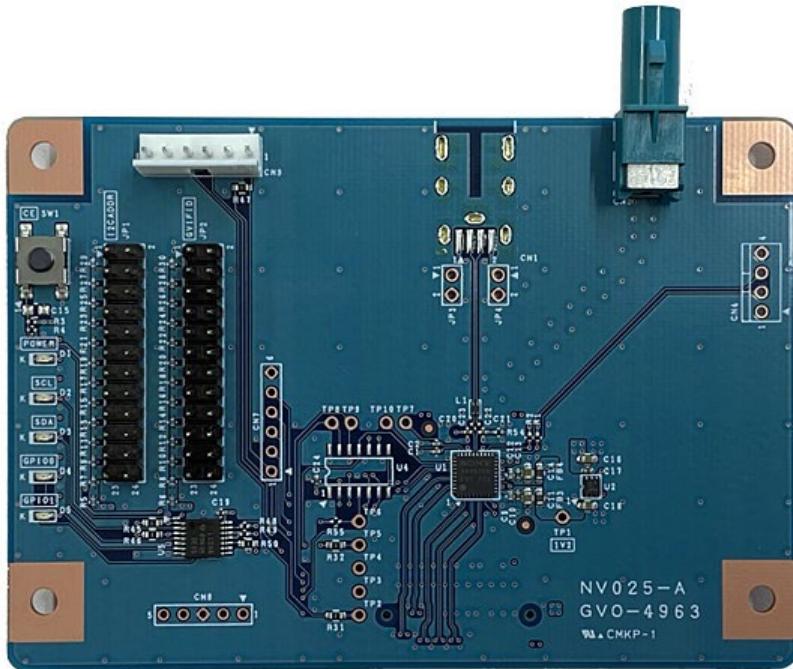
Main Connector Layout Diagram



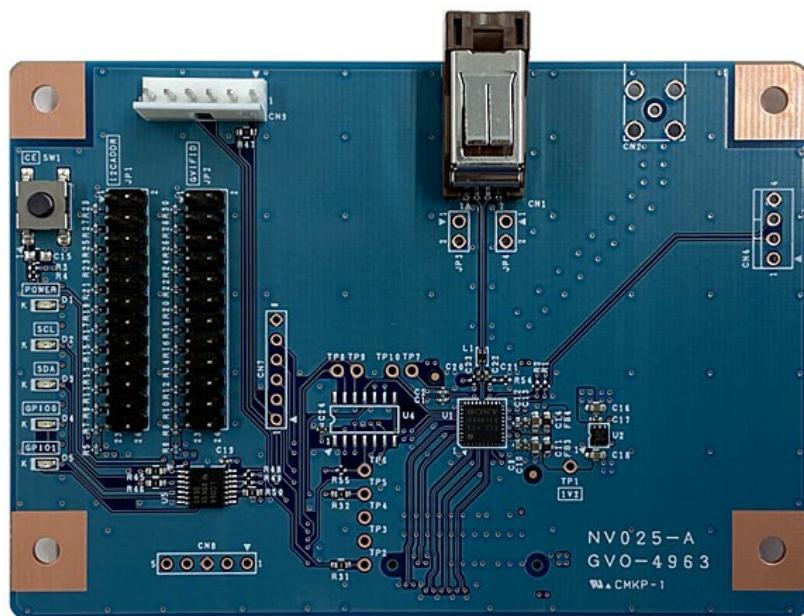
- Only the main connectors are shown.
- CN4 and CN8 are not implemented.

2.2 Shape of The Board

GVO-4963-F



GVO-4963-M



3. Details

3.1 Connectors List

CN#	Mounted State	Description	Model Number
CN1	Only -M	GVIF2 output (differential)	MX79A04HQ2
CN2	Only -F	GVIF2 output (coax)	FA1-NCRP-PCB-8
CN3		For SV boards connection	QTH-030-01-L-D-A
CN4	Un-mounted	I2C input and output connector	171825-4
CN7	Un-mounted	GPIO input and output	A2-6PA-2.54DSA(71)
CN8	Un-mounted	For writing PIC ICSP	A2-5PA-2.54DSA(71)
CN9		Expansion connector	171825-6

- This mounting state apply to NV025-A / GVO-4963-F/M.
- The expansion connector (CN9) is for board-to-board communication in multi board output systems and for future expansion.
- The I2C input and output connector (CN4) is directly connected to the I2C bus of the serializer IC (CXD4963).

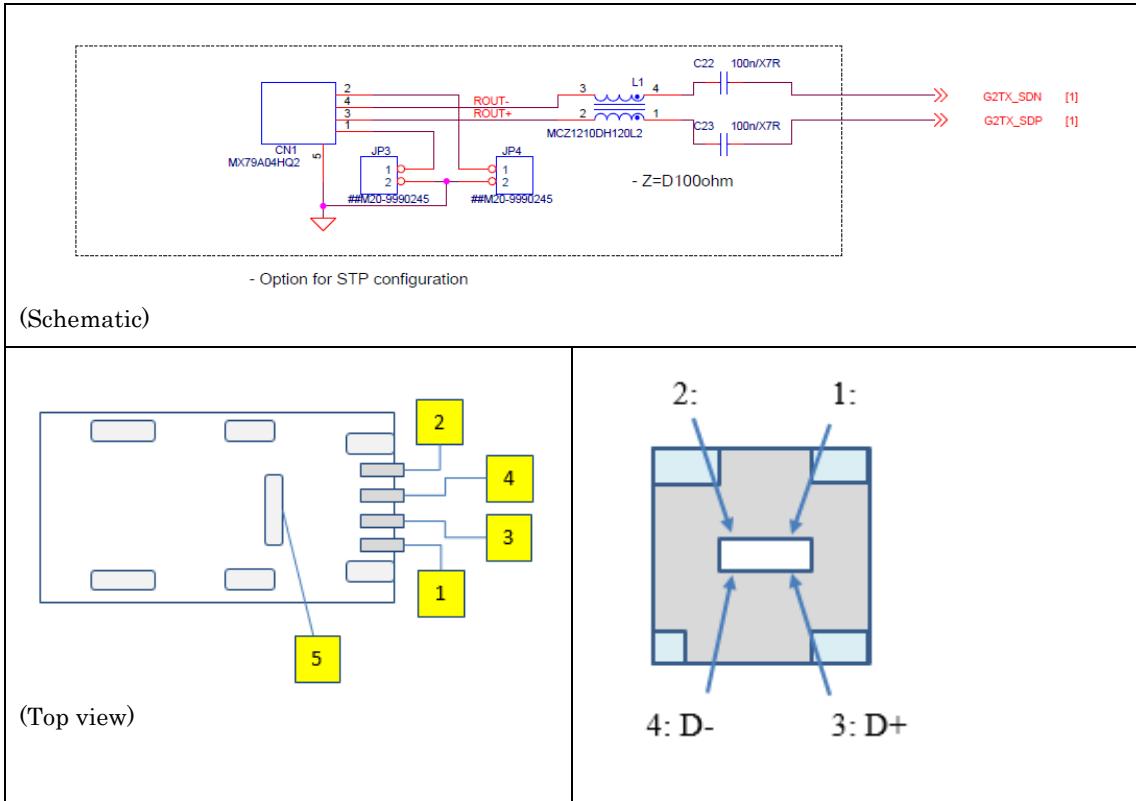
3.2 Connectors Details

The following is top view images (rough drawing) and pin assignments (excerpt from the schematic) of the connectors on the board.

(Pin assignment legend)

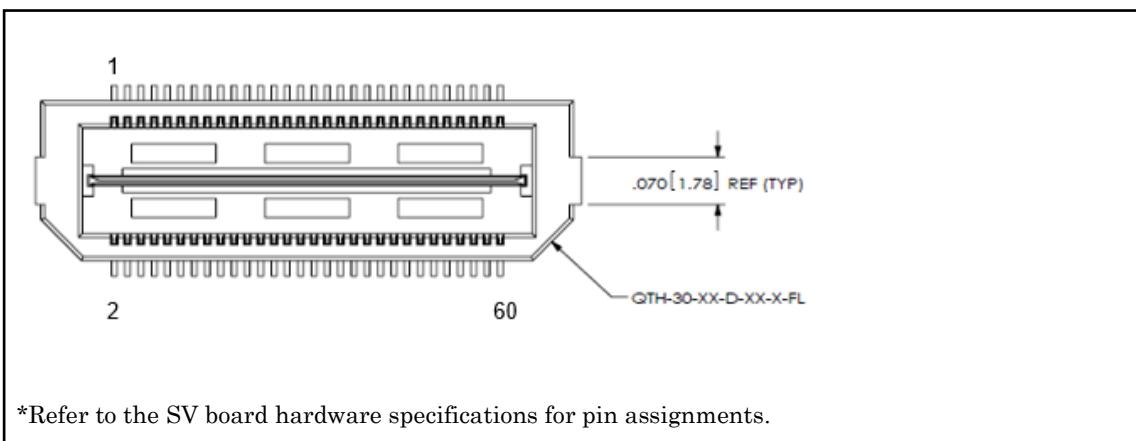
Name	Description
VDDIO	IO power supply (Directly connected to CN3).
SVM_GPIO0 - 7	Connected to GPIO0-7 of CN3. When R33-R37 are mounted, SVM_GPIO4-7 are connected to GIO0-3 of the CXD4963.
SER_SCL / SER_SDA	I2C signal line (Connected to CXD4963 and CN3).
P0_FSIN	Connected to pin 2 of the CN3 (SVM_GPIO0).
P3_FSOUT	Connected to pin 10 of the CN3 (SVM_GPIO3).

• CN1 (MX79A04HQ2)

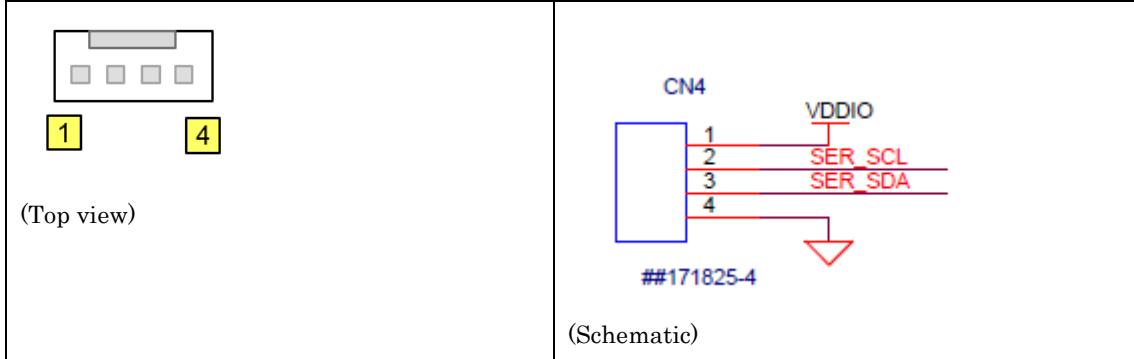


- Pin assignment 4: D- / 3: D+ is fixed. Pins 1 and 2 can be connected to GND by JP3 and JP4.

• CN3 (QTH-030-01-L-D-A)

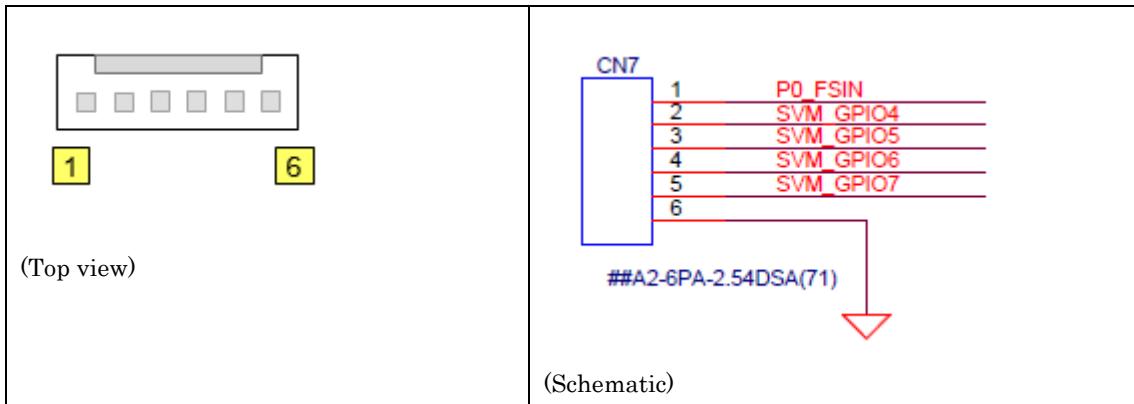


• CN4 (171825-4 / TE Connectivity)



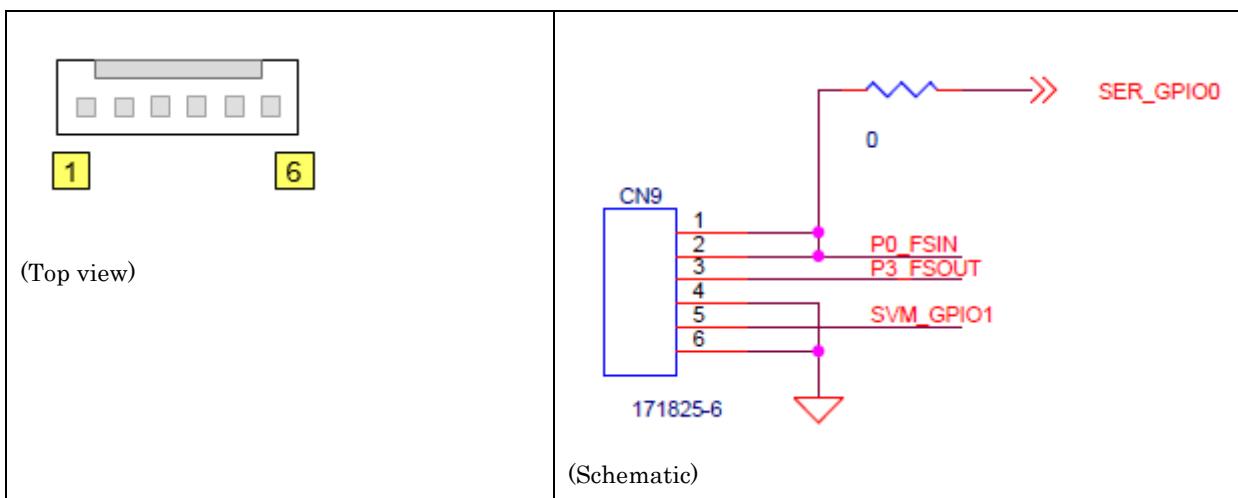
- Directly connected to the I2C bus of the CXD4963.
- This is not mounted.

• CN7(A2-6PA-2.54DSA(71) / HRS)



- This is not mounted.

• CN9(171825-6 / TE Connectivity)



3.3 Switch

The SW1 is mounted as a reset switch. When the SW1 is pushed, the CE pin of the CXD4963 is set to the “L” state.

3.4 Jumper Settings

Two jumpers (JP1, JP2) and a reset switch are mounted for setting the CXD4963. The I2C address and GVIFID of the serializer are set according to the state of the jumpers.

- **JP1**

JP1 is a jumper that specifies the I2C address of the CXD4963. Please select one of the options in the table below.

Short Circuit Pin	I2C Address (7 bit)
1-2	0b0100000 (0x20)
3-4	0b0100001 (0x21)
(Omission)	
19-20	0b0101001 (0x29)
21-22	0b0101010 (0x2A)

- The factory default is 1-2 short circuit.

- **JP2**

JP2 is a jumper that specifies the GVIFID of the CXD4963. Please select one of the options in the table below.

Short Circuit Pin	GVIFID
1-2	0b01000000 (0x40)
3-4	0b01000001 (0x41)
(Omission)	
19-20	0b01001001 (0x49)
21-22	0b01001010 (0x4A)

- The factory default is 1-2 short circuit.

3.5 LED Indicator

LED#	Name	Description
D1	POWER	When power (3.3V) is supplied, lights up.
D2	SCL	When the SCL pin of the CXD4963 I2C bus is L, lights up.
D3	SDA	When the SDA pin of the CXD4963 I2C bus is L, lights up.
D4	GPIO0	When the GIO0 pin of the CXD4963 is H, lights up.
D5	GPIO1	When the GIO1 pin of the CXD4963 is H, lights up.

3.6 Power Supply

The power for the serializer IC CXD4963 is supplied from the SV board via the CN3. The core power supply and IO power supply are 1.8V, and the serializer is powered by a 1.8V regulator (LDO) on this GVO-4963 board. The IO supply voltage supports 1.8V / 3.3V.

3.7 GPIO

The GIO0 – 10 pins of the serializer IC CXD4963 are connected to GPIO4 - 14 of CN3 (see schematic for pin numbers) via a jumper resistor, allowing control from the SV board. The GPIO connection can be disconnected by leaving R33-44 unmounted.

3.8 MIPI Signal Input Assignment

The MIPI signal input of the CXD4963 has 4 data lanes and 1 clock lane connected to CN3. The connection assignment is fixed as shown in the table below.

CXD4963	CN3 (SV board)
RX_AN	MIPI_D4_N
RX_AP	MIPI_D4_P
RX_BN	MIPI_D2_N
RX_BP	MIPI_D2_P
RX_CN	MIPI_CLK1_N
RX_CP	MIPI_CLK1_P
RX_DN	MIPI_D3_N
RX_DP	MIPI_D3_P
RX_EN	MIPI_D1_N
RX_EP	MIPI_D1_P

The MIPI receiver lane assignment of the CXD4963 is required for operation of this board. The registers of CXD4963 should be set as shown in the table below.

Address	Register	Value	Description
0x69 (b7)	MIPI_RX_DATA_MODE	0x1	Data mode 1
0x69 (b6-4)	MIPI_RX_CLK_MODE	0x2	Clock mode 2
0x6A (b0)	MIPI_RX_PN_SWAP	0x0	Same as pin name
0x6B (b3-0)	MIPI_RX_DATA_EXTENDED_MODE	0x2	Data extension mode 2

4. Specifications

Item	Value	Description
Board Dimensions	101.6 x 71.0 mm	Value not including connectors.
Serializer Power Supply	DC +3.3V	Supplied from the power supply (3.3V) of SV board via CN3. Stepped down to 1.8V by the internal LDO.
IO Voltage	DC +1.8V or +3.3V	Set to +3.3V for PIC programming.
Image Input	MIPI CSI-2 1-4 Lanes + CLK	Input from CN3. Refer to the CXD4963 standard for details on supported formats. Connector interface conforms to SV board.
Image Output	GVIF2 Max: 4.8Gbps	Output from connector CN1 or CN2.
Serial Communication	I2C Communication	I2C bus outputs to CN3 and CN4. A PIC microcontroller (PIC16LF1825T) mountable pattern is available for emulating the I2C response.

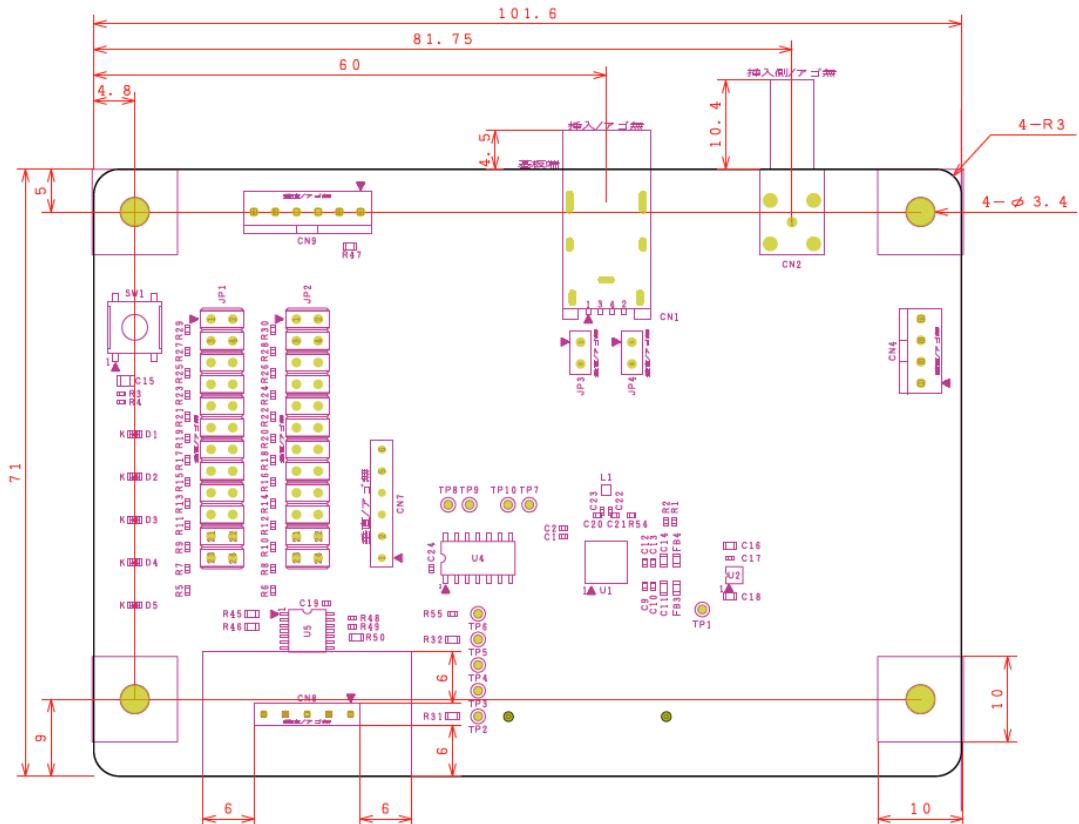
- The above specifications apply only to the NV025-A / GVO-4963-F / -M.

- When connecting to our SV board, it must be set to the Continuous Clock.

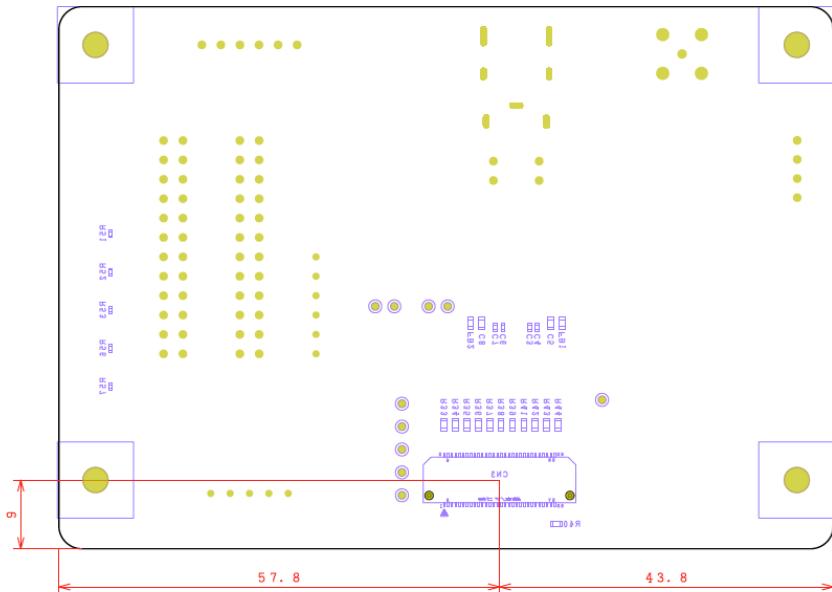
5. Appendix

5.1 Figure of Board Dimensions

(Top Side / Part View)



(Bottom Side / Part View)



5.2 PIC Microcontroller Peripheral Circuit Diagram

