MIPI Monitoring Board

[SVM-06 rev.1.4]

Hardware Specification

Rev.1.1

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	9. Apr., 2020	New File（Equivalent to Japanese version 1.4）	H. Suzuki
1.1	27. Dec., 2024	Revised translation (Equivalent to Japanese version 2.8)	R. Sugo

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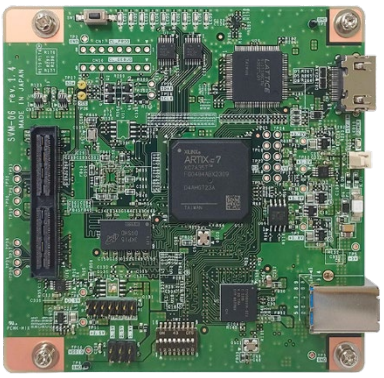
1. Overview



This document outlines the hardware specifications of the **"SVM-06"** to convert the MIPI CSI-2 video signals from a target device to HDMI or USB 3.0.

The board operates according to the mode specified by the DIP switch (SW2). There are three modes, **HDMI mode, UVC mode and Updater mode**. Additionally, custom modes are available, such as a vendor output mode similar to our SVP-01-VEN and a MIPI output mode similar to our SVO-03-MIPI.

In HDMI mode, the SVM-06 outputs images from target devices such as image sensors and displays them on an HDMI monitor in real-time, enabling smooth verification and evaluation. This board is equipped with a 300 MHz TMDS HDMI transmitter and supports video resolutions up to 4K at 30fps or 1080p at 120fps. Furthermore, since the USB port operates in UVC mode, it is possible to capture the video with a PC via USB3.0 while simultaneously displaying the video on HDMI monitor.

In UVC mode, the SVM-06 captures video and functions as a UVC (USB Video Class) compliant device, enabling you to evaluate target devices and develop algorithms on various operating systems such as Windows and Linux. Uncompressed video data can be transmitted at a maximum bandwidth of 3 Gbps, as the data is transferred via USB3.0. Being a UVC compliant device without the need for additional device drivers, it can be easily integrated with third-party software such as OpenCV and ROS. Although HDMI mode provides the same functionality as UVC mode, UVC mode is more power-efficient. Therefore, when only the USB port is in use, it is recommended to use UVC mode.

In Updater mode, you can update the firmware and FPGA via USB. This board does not support updates in HDMI or UVC modes, so make sure to switch to Updater mode when performing an update.

1.1. SVM-06 Functions

HDMI mode: MIPI Video Signals -> HDMI Conversion (Simultaneous output to USB3.0)

UVC mode: MIPI Video Signals -> USB3.0 (UVC) Conversion

Updater mode: Update the board firmware

1.2. Specifications (HDMI Mode)

Power: USB Bus Supply (External power input applicable) / +5V 0.9A typ.

Input Standards: MIPI CSI-2 Video Signal (Data 1 - 4 lanes)

- Data rate per lane: Max. 1.5 Gbps.
- Effective pixel data rate: Max. 5.2 Gbps (YUV422 8bit) preliminary.

Input Resolution: Max. (Width x Height) pixel

- Width = 8190 or 32000 x (number of data lanes) / (bits per pixel), whichever is smaller.
- Height = 4095

Input Pixel Format: YUV4:2:2 (8bit), Raw10, Raw12, RGB24

Output (1): HDMI Connector (YUV4:2:2 8bit, YUV4:4:4 8bit or RGB24)

Output (1) Resolution: 1280x720 / 1920x1080 / 2560x1440 / 3840x2160 / For custom, max. 8190x4095

- The input image can be cropped to any desired region.

Output (1) Frame Rate: 30 FPS / 60 FPS / Custom resolutions can support any frame rate.

- The 3840x2160 resolution is supported only at 30 FPS.

Output (1) Data Rate: Max. 7.2 Gbps (Theoretical value, Equipped with 300MHz TMDS transmitter)

Output (2): USB 3.0

- The max resolution is the same as in UVC mode, but the automatic frame rate adjustment function is not available.

- In the case of Raw input, the image is output as a monochrome image (Pixel-by-Pixel) in HDMI mode.

- If you want Raw input and color output, please contact us.

- If you want to know how to set the custom resolution, please contact us.

1.3. Specifications (UVC Mode)

Power: USB Bus Supply (External power input applicable) / +5V 0.7A typ.

Input Standards: MIPI CSI-2 Video Signal (Data 1 - 4 lanes)

- Data rate per lane: Max. 1.5 Gbps
- Effective pixel data rate: Max. 5.2 Gbps (YUV422 8bit) preliminary.

Input Resolution: Max. (Width x Height) pixel

- Width = 8190 or 32000 x (number of data lanes) / (bits per pixel), whichever is smaller.
- Height = 4095

Input Pixel Format: YUV4:2:2 (8bit), Raw8, Raw10, Raw12, Raw16, Raw20, RGB24

Output: USB 3.0 (USB 2.0 is possible if the resolution is about VGA)

USB Device Class: USB Video Class (UVC)

Output Through Rate: Max. 3.0 Gbps

- With automatic frame rate adjustment, it supports input signals faster than the USB bandwidth.
- Actual throughput depends on the environment such as the host controller.

Output Resolution: Same as input resolution

- The input image can be cropped to any desired region.

Output Frame Rate: Any value

Output Pixel Format: YUV4:2:2, RGB24

- In the case of Raw input, all data is output by assigning it to the pixel format YUV 4: 2: 2. Our capture software (NVCap) enables monochrome and color display.

1.4. Board Specification Table

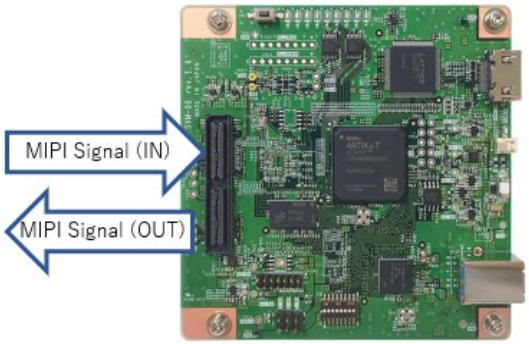
Item		Content	Remark
Video Input Interface		MIPI D-PHY CSI-2 video signal FPD-Link III / GMSL / GVIF2 (When connecting with our deserializer boards.)	Supports Non-Continuous / Continuous Clock. Standard specification: 4 lanes + 1 clock lane are available. For custom, max. 8 data lanes + 2 clock lanes are available. 2 system inputs or 1 input + 1 output are available.
Video Output Interface		UVC (USB Video Class) / HDMI 1.4	USB supports Windows / Ubuntu
Input Resolution		Max. 8190 x 4095 pixel Within 6.0 Gbps	The range of widths that can be input depends on the number of lanes. The maximum data rate during operation is approximately 5.3 Gbps.
Output Resolution		Max. 8190 x 4095 pixel (UVC mode) Within 3.0 Gbps (HDMI mode) Within 3840 x 2160, (less than 30 fps)	(Standard resolution in HDMI mode) 1280 x 720 / 1920 x 1080 / 2560 x 1440 / 3840 x 2160 In UVC mode, make sure that the effective data rate in the frame is within 3.0 Gbps.
Sync Signal		FS / FE	
MIPI Data Lane		1, 2, 3, 4 lanes	
Data Rate Per Lane		Max. 1500 Mbps	Data rate per lane = Clock lane frequency x2
Supported Pixel Formats		YUV4:2:2 8bit / RGB24 / Raw8 / Raw10 / Raw12 / Raw16 / Raw20	Raw8, Raw16 and Raw20 are supported only in UVC mode. Raw8 grayscale output is not supported.
Other IF	I2C	1 system	SCL frequency 100 / 200 / 400 kHz
	GPIO	16 bits	IN / OUT can be switched for each bit.
Input Power		+5V (±5%)	Use either USB bus power or 2-pin connector.
Output Power		VDDIO output (1.8V, 2.5V, 3.3V) 5V, 3.3V, 1.2V output	Since it is shared with the internal power supply, so we recommend to use a current of 150 mA or less for each. The current ratings are 800mA (1.8V, 2.5V, 3.3V), 500mA (1.2V, 5V).

Other Functions	Test pattern output Image clipping Automatically transmit I2C at startup (ROM startup)	Virtual Channel and VCX Embedded Line are supported individually.
Interface Connector	120pin (QSH-060-01-L-D-A)	It is also possible to use as a 60-pin connector.
FPGA	Artix-7 (XC7A35T) CrossLink (LIF-MD6000)	
Frame Memory	256MB (DDR3 SDRAM)	
USB3.0 Chip	Infineon EZ-USB FX3	
HDMI Chip	SiI1136	
Board Dimensions	101.6 x 101.6 x 25.7 [mm]	Length x Width x Height
Attached Software (Windows)	NVCap SVMCtl SVMUpdater	
Examples of Supported Deserializer Board	FPI-954-F GMI-9286-F GMI-9288-F GVI-4960-F and so on.	

1.5. MIPI CSI-2 Data Processing Specifications

- Short Packets FS/FE are used for frame detection. LS/LE are not used, but it does not matter if LS/LE are included in the input data.
- Only payload data is sent to USB and HDMI. Packet header and packet footer contents are not sent.
- ECC and CRC errors are ignored.
- Virtual Channel VC = 0-3 are supported. Please contact us if you need support VCX.
- The behavior when data exceeding the board's specifications is input to the SVM-06 is undefined.

1.6. Operation by Daisy Chain Connection

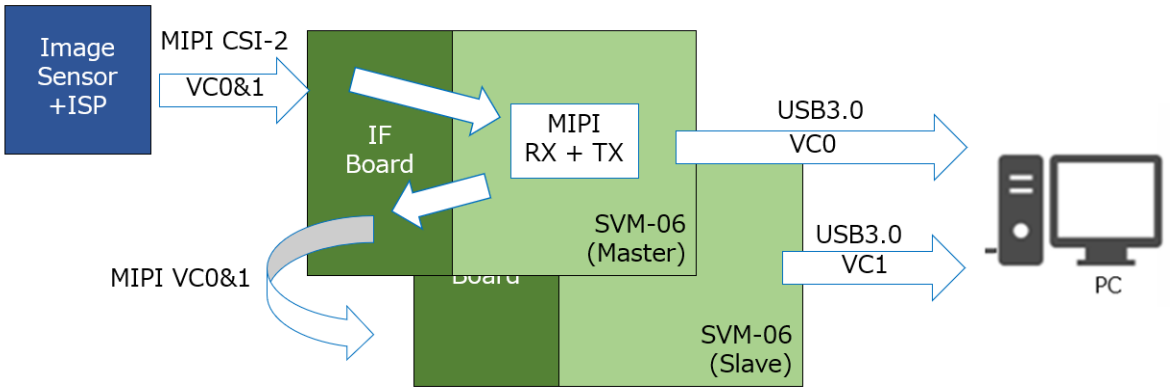


SVM-06 has 4 lanes x 2 systems MIPI input/output ports. Therefore, MIPI signals input from one port can be output from the other port.

As shown in the figure below, the Daisy Chain connection allows a single MIPI signal containing multiple Virtual Channels to be input to multiple boards, with each Virtual Channel assigned to a separate USB port for import to a PC.

Since the Daisy Chain output side has the same specifications as the input side, it can output videos at up to 6 Gbps, exceeding the performance of USB 3.0.

It is possible to import video signals exceeding the USB3.0 bandwidth by using the clipping function to reduce the transfer rate per board and using multiple boards through Daisy Chain connection.



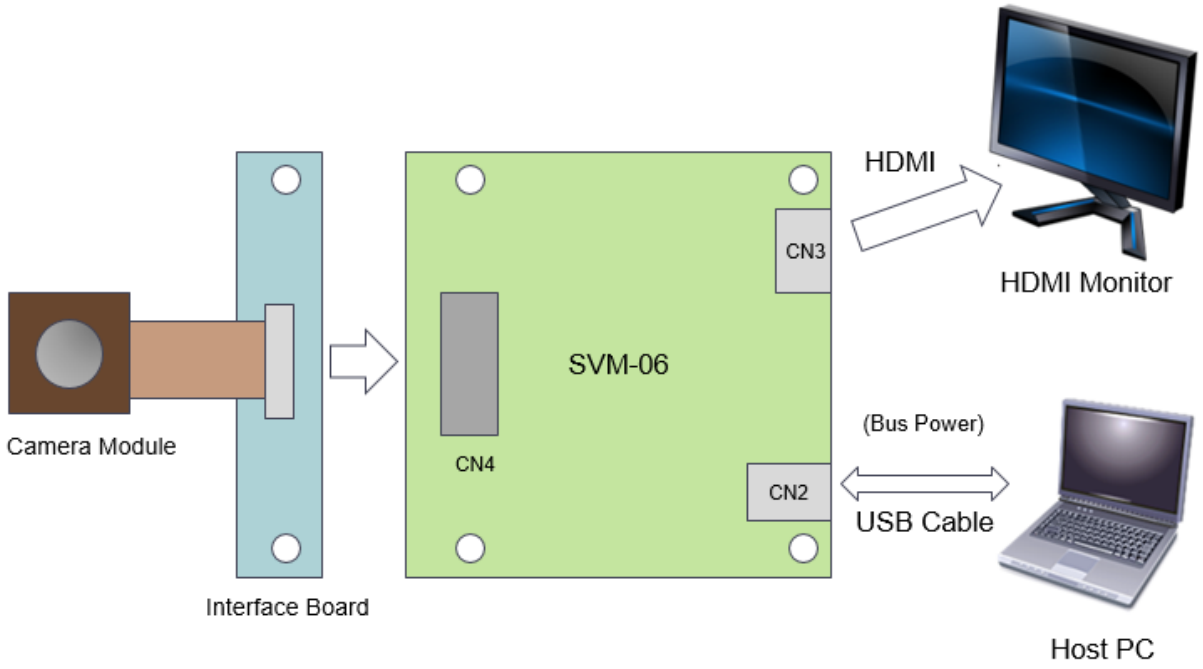
The Daisy Chain function is not implemented in the standard version of SVM-06. It is necessary to manufacture an interface board to connect the Daisy Chain output signal to another SVM-06.

In addition, the CrossLink FPGA in the SVM-06 must be updated to use. Please contact us for more details.

2. HDMI Mode Operation Details

This chapter describes HDMI mode (MIPI input, HDMI output). When the power is turned on with the DIP switch on the board set to 8: OFF and 7: OFF, it starts in HDMI mode.

2.1. Connection Example in HDMI Mode



2.2. Input Settings

There are three input settings that must be set in HDMI mode: number of MIPI lanes, resolution setting, and clipping setting.

Since the number of MIPI lanes is set with the DIP switch, please refer to the DIP switch setting described later. The resolution setting and clipping setting are set with our software ”SVMCtl” via USB(PC). The settings are saved in the SPI-ROM on the board, and they are reflected at startup.

The resolution setting is specified at "UVC Resolution" of "SVMCtl", so set the resolution of the input image or after clipping.

The clipping setting is used to enable the clipping function, which outputs only a portion of the input image. The clipping resolution must match the HDMI output resolution.

For details, please refer to the “SVMCtl Software Manual”.

2.3. Output Settings

The settings for HDMI output are configured via the DIP switch on the board and our software SVMCtl. The output resolution can be selected from several built-in standard resolutions or from a custom resolution that can be freely set by the user.

To output in standard resolutions (720p, 1080p, 1440p, 2160p = 4K), the settings can be configured by adjusting the DIP switch. Ensure that the resolution and frame rate match those of the monitor or target device. The output format is configured via SVMCtl.

To output in a custom resolution, resolution timing data can be written from a PC to the board using SVMCtl, allowing HDMI output at any resolution up to approximately 8000x4000. The output format supports YUV4:2:2 8bit, YUV4:4:4 8bit or RGB 24bit. Timing data can be created using the software "SVOGenerator", which is designed for our MIPI Generator board.

When custom timing data is written, the settings via DIP switches #5 and #6 are ignored. To re-enable the DIP switch resolution settings, delete the custom resolution data via the SVMCtl.

2.4. Power Supply

SVM-06 consumes about 900 mA on the 5V line when outputting the built-in test pattern without a target connection in HDMI mode. When a target is connected, the power consumption may be higher, so please use a sufficient AC adapter or a USB cable. In UVC mode, the power consumption is about 750 mA.

2.5. USB Bus Power Supply

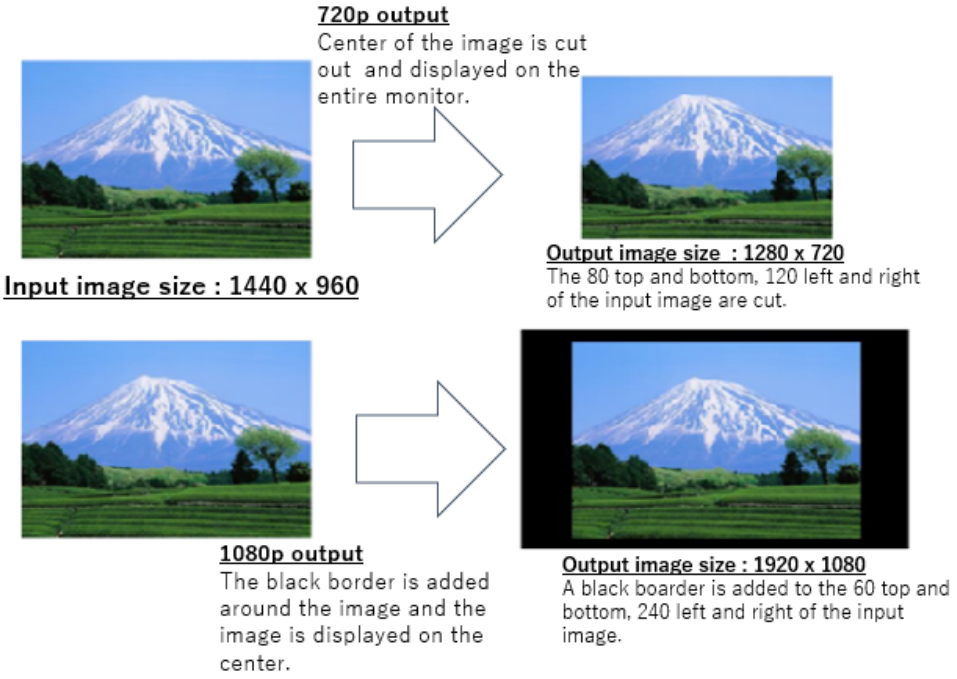
SVM-06 can be powered by USB from a PC, but the USB specification has limitations: the maximum current is 500 mA for USB 2.0 ports and 900 mA for USB 3.0 ports. Therefore, we cannot guarantee proper operation when using USB bus power from a PC.

2.6. Operation When Input and Output Resolutions are Different

When the input resolution is larger than the output resolution and the clipping setting is disabled, the center of the input image is automatically cropped for output. With the clipping setting enabled, the image is displayed according to the specified settings.

On the other hand, when the input resolution is smaller than the output resolution and the clipping setting is disabled, the input image is displayed in the center of the output screen with a black border around it. With the clipping setting enabled, the image is displayed according to the specified settings, also with a black border around it. The function to enlarge or shrink the image is not available.

Clipping Setting	Input resolution is larger than output	Input resolution is smaller than output
Enabled	Crop with the clipping settings	Crop with the clipping settings with a black border around it
Disabled	Crop the center of the input image	Display the input image in the center of the output screen with a black border around it



2.7. Processing at RAW Input

For raw input formats in HDMI mode, SVM-06 supports Raw10 and Raw12 format inputs. However, the image is output as a monochrome image, with one output pixel for each input pixel (dot-by-dot). Only the upper 8 bits are output and the lower bits are truncated. Raw development functions (such as de-mosaic and color display) are not supported.

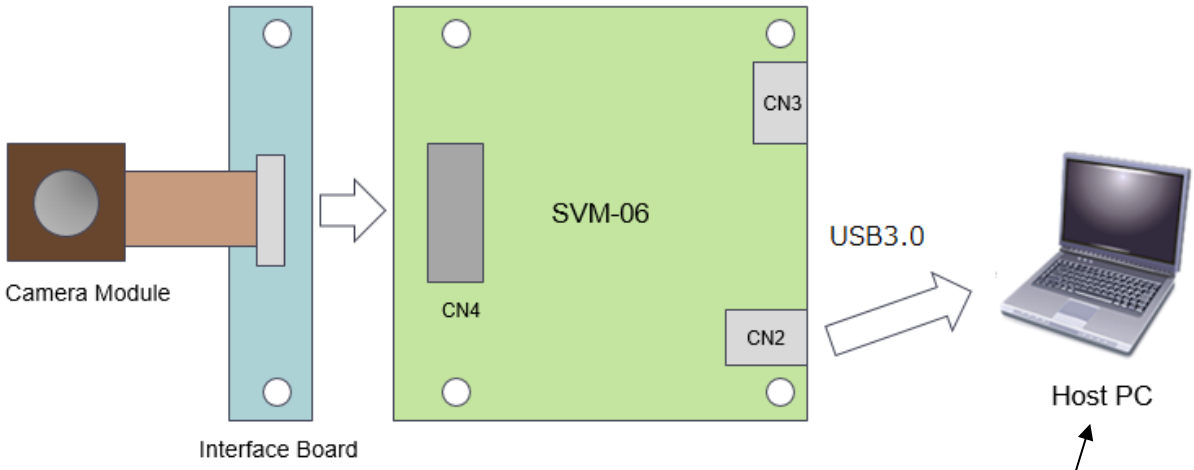
2.8. USB Simultaneous Output

In HDMI mode, SVM-06 can output images to both HDMI and USB simultaneously. By default, video format settings, including clipping settings, are shared between both outputs. The USB output operates in the same way as UVC mode. However, it is possible to apply separate settings for UVC and HDMI modes by directly modifying the FPGA register. Please contact us for more details.

3. UVC Mode Operation Details

This chapter describes UVC mode (MIPI input, USB output). When the power is turned on with the DIP switch set to 8: ON and 7: OFF, it starts in UVC mode.

3.1. Connection Example in UVC Mode



DirectShow Capture Software

3.2. Format Settings

Certain settings must be configured in UVC mode: resolution, frame rate, and output pixel format, along with the MIPI lane count and clipping settings shared with HDMI mode. Since the MIPI lane count is set with the DIP switch, please refer to the DIP switch setting described later.

The clipping setting enables the clipping function, which outputs only a portion of the input image. This setting is set with SVMCtl, and saved in the SPI-ROM.

The resolution and frame rate are also set with SVMCtl. Set these parameters according to the input video. If using the clipping function, you should set the resolution to match the clipped resolution. The output pixel format should also match the input pixel format of the MIPI signal. Generally, UVC supports three types of uncompressed video pixel formats: UYVY, YUY2, and RGB24. For other output pixel formats, please feel free to contact us.

3.3. Automatic Frame Rate Adjustment Based on USB Transfer Bandwidth

SVM-06 supports a USB3.0 transfer bandwidth up to 3 Gbps (theoretical), but it is capable of handling input signals with higher data rates. The actual available USB bandwidth depends on the host controller and operating environment.

By enabling the automatic frame rate adjustment function, the output frame rate is automatically adjusted to match the effective USB bandwidth. This allows the capture of video signals with throughput exceeding the USB bandwidth. To enable this function, select “Auto” for the “Decimation” setting in SVMCtl. This function is required when input video signals have a peak bandwidth exceeding the USB bandwidth. Note that enabling this function increases data latency.

3.4. Initial Setting Procedure

In UVC mode, initial settings must be configured when first using the SVM-06, based on the specifications of the target device. If the settings do not match the specification of the target device, proper image capture may not be possible.

1. Set Target Power Voltage (VDDIO)

   Before connecting the target device, ensure that VDDIO is set to match the IO voltage of the target device. VDDIO can be switched using the jumper pin (JP1), with the default setting at 3.3V.

2. Set DIP Switch

   The DIP switch should be set based on the MIPI lane count of the target device. The default setting is 4 lanes. Refer to Section 7.2 for the detail of the DIP switch settings.

3. Initial Setting from PC

   Initial settings such as resolution and pixel format must be configured from a PC. These settings can be set using the SVMCtl software. For detailed instructions on operating SVMCtl, please refer to the "SVMCtl Software Manual."

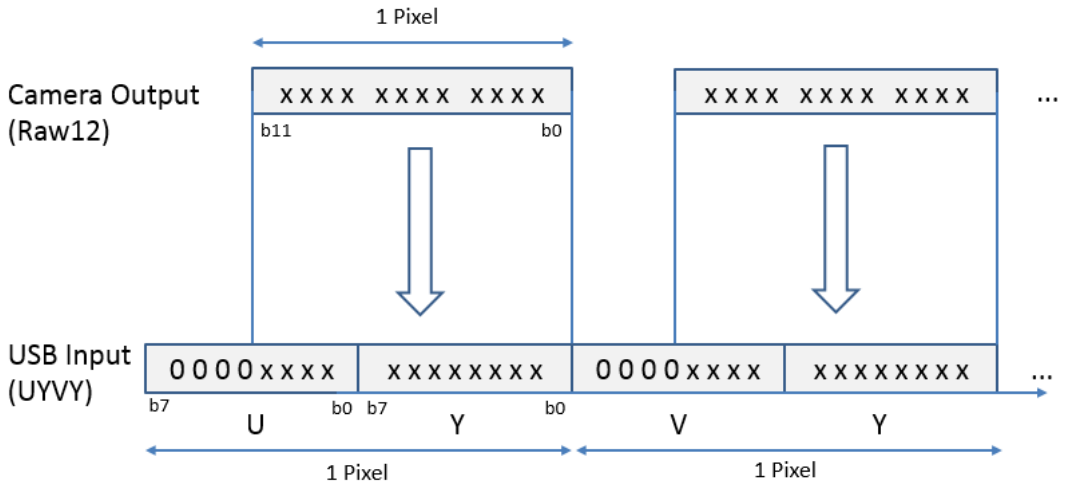
The default settings follow the settings described in the inspection report. The standard settings are as follows:

Resolution: 1920 x 1080
Frame Rate: 30 FPS
Color Space: UYVY

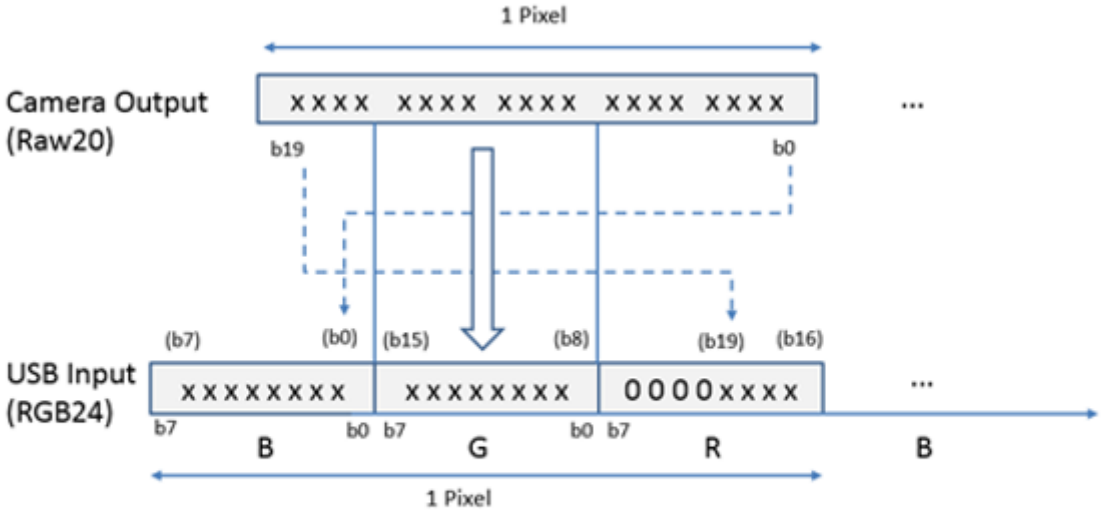
- SVMCtl may be updated as needed. The latest version can be downloaded from our website.
- This board is recognized by a PC as a device named "SVM-06".
- If a device ID is assigned via SVMCtl, the ID number is displayed in parentheses after the device name.

3.5. Processing on RAW Input

In UVC mode, SVM-06 supports Raw 8, Raw10, Raw12 and Raw20 for Raw input formats. However, the UVC standard does not support Raw format. For Raw8 to Raw12, the input data is extended to 16 bits wide, with the upper bits set to 0 before being output to the PC. To capture video with Raw format, you should pack it into a 16-bit/pixel format by specifying UYVY in the pixel format setting. After that, Raw image processing can be performed using software on the host PC. Additionally, Raw input can be output as a monochrome YUV 8bit format by additional settings with SVMCtl.



In the case of Raw20, the input data is treated as 24bits wide, with the upper bits set to 0 before being output to the PC. The data is packed into a 24bit/pixel format by specifying RGB24 in the pixel format setting, after which Raw image processing can be performed using software on the host PC. Please refer to the "SVMCtl Software Manual" for the detailed settings.

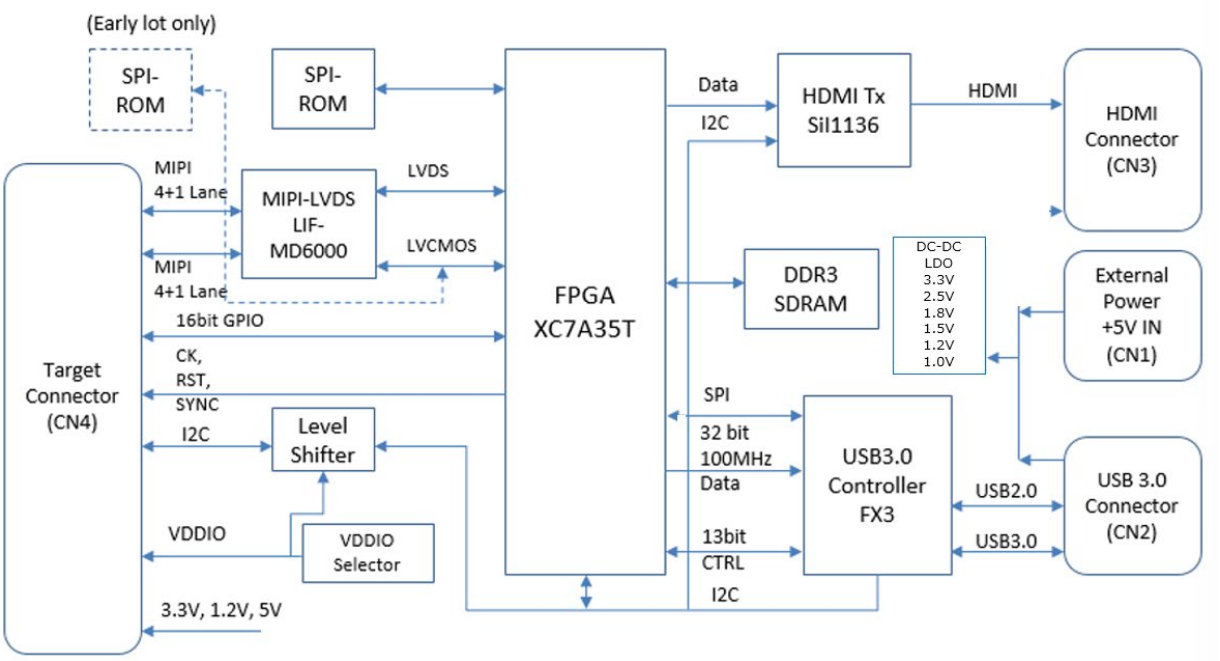


The host side treats the data as RGB24 and the upper bits are set to 0. (Bit rate is 6/5 times)

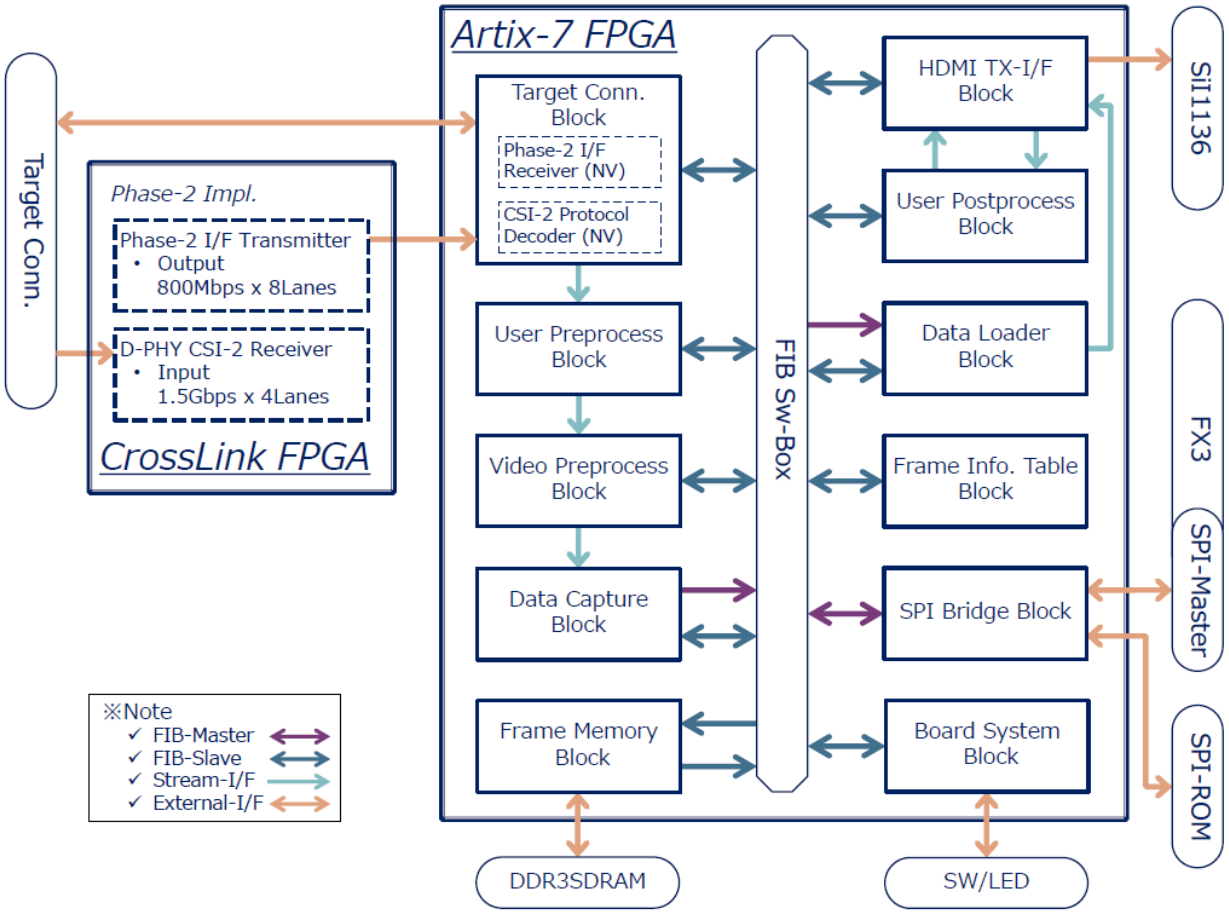
4. Block Diagram of SVM-06

A schematic block diagram of SVM-06 is shown below.

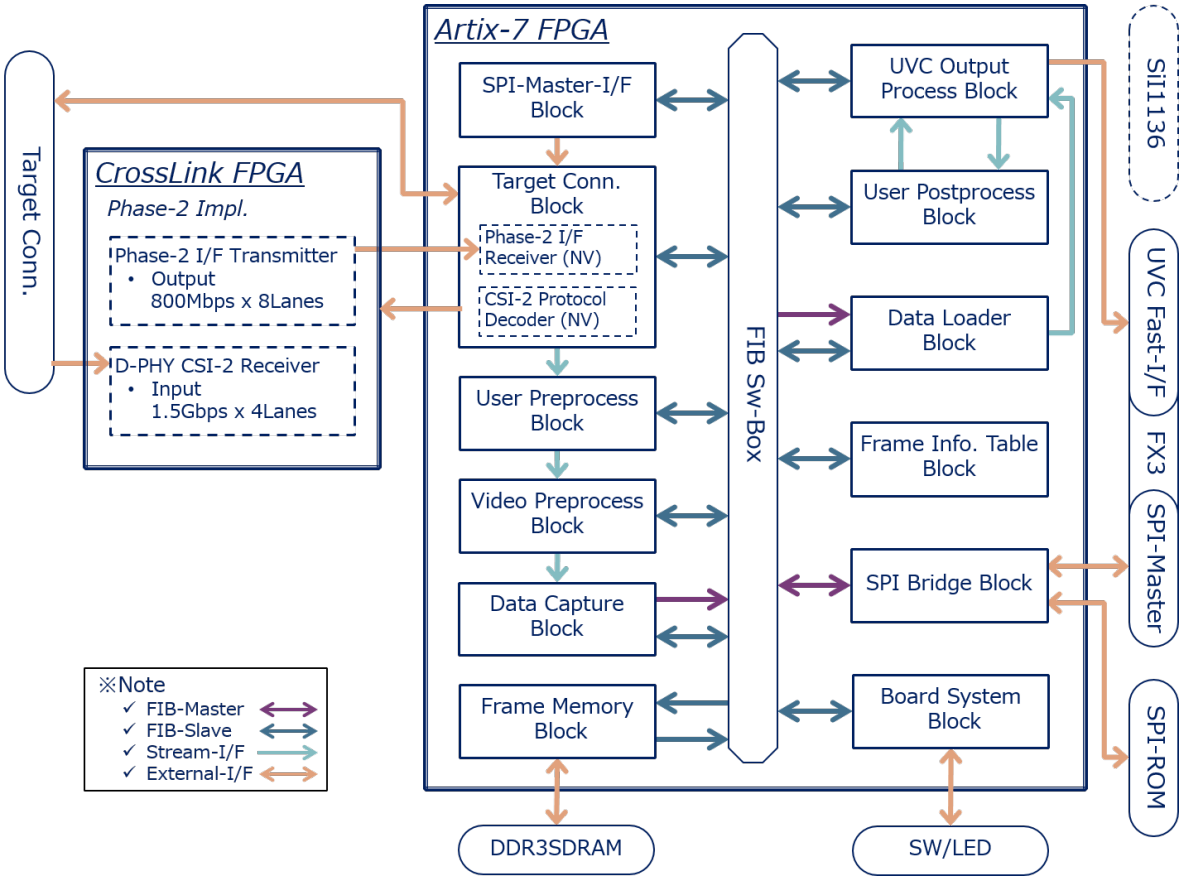
4.1. Block Diagram



4.2. FPGA Internal Block Diagram in HDMI Mode



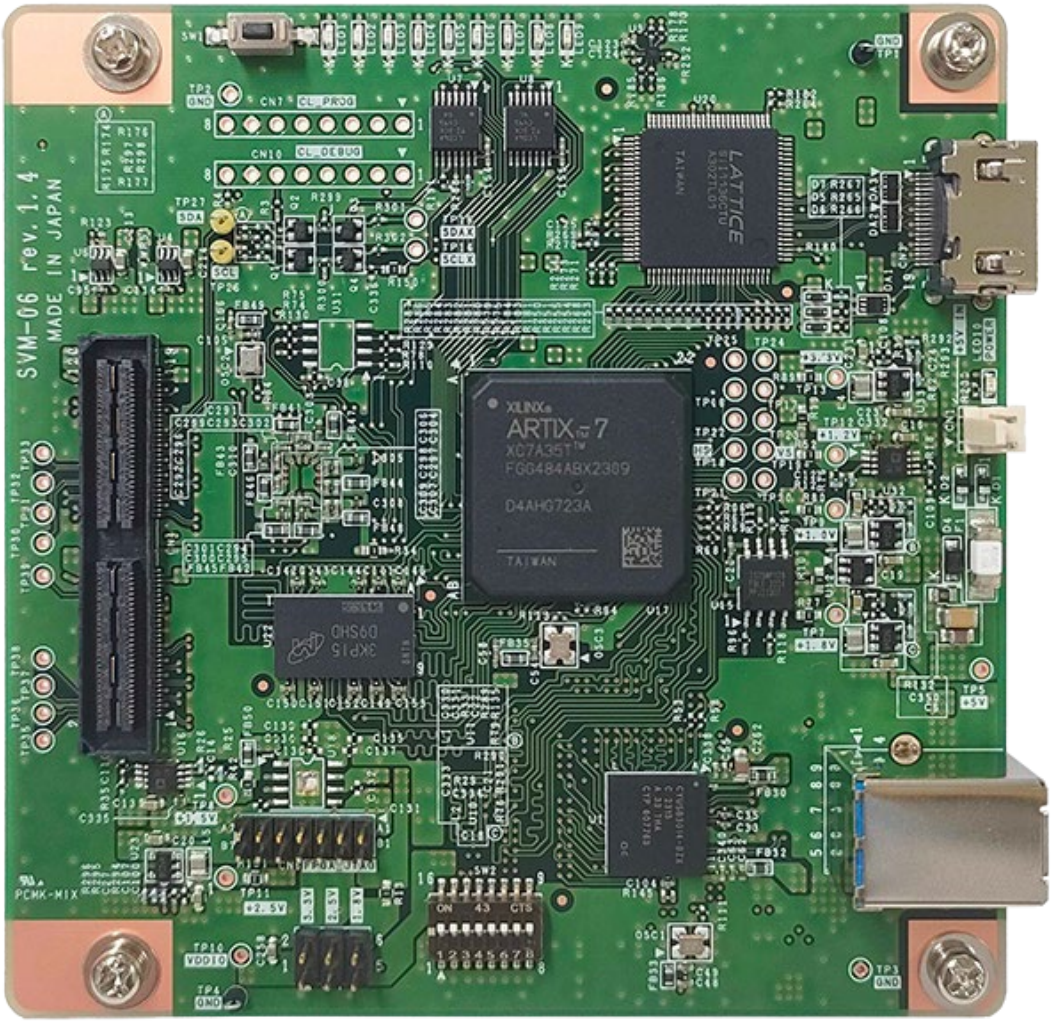
4.3. FPGA Internal Block Diagram in UVC Mode



5. The Shape of The Board

The photo and the picture of the outline of SVM-06 are shown below.

5.1. The Photo of The Board (rev.1.4)



5.2. Difference Between Rev.1.3 and 1.4

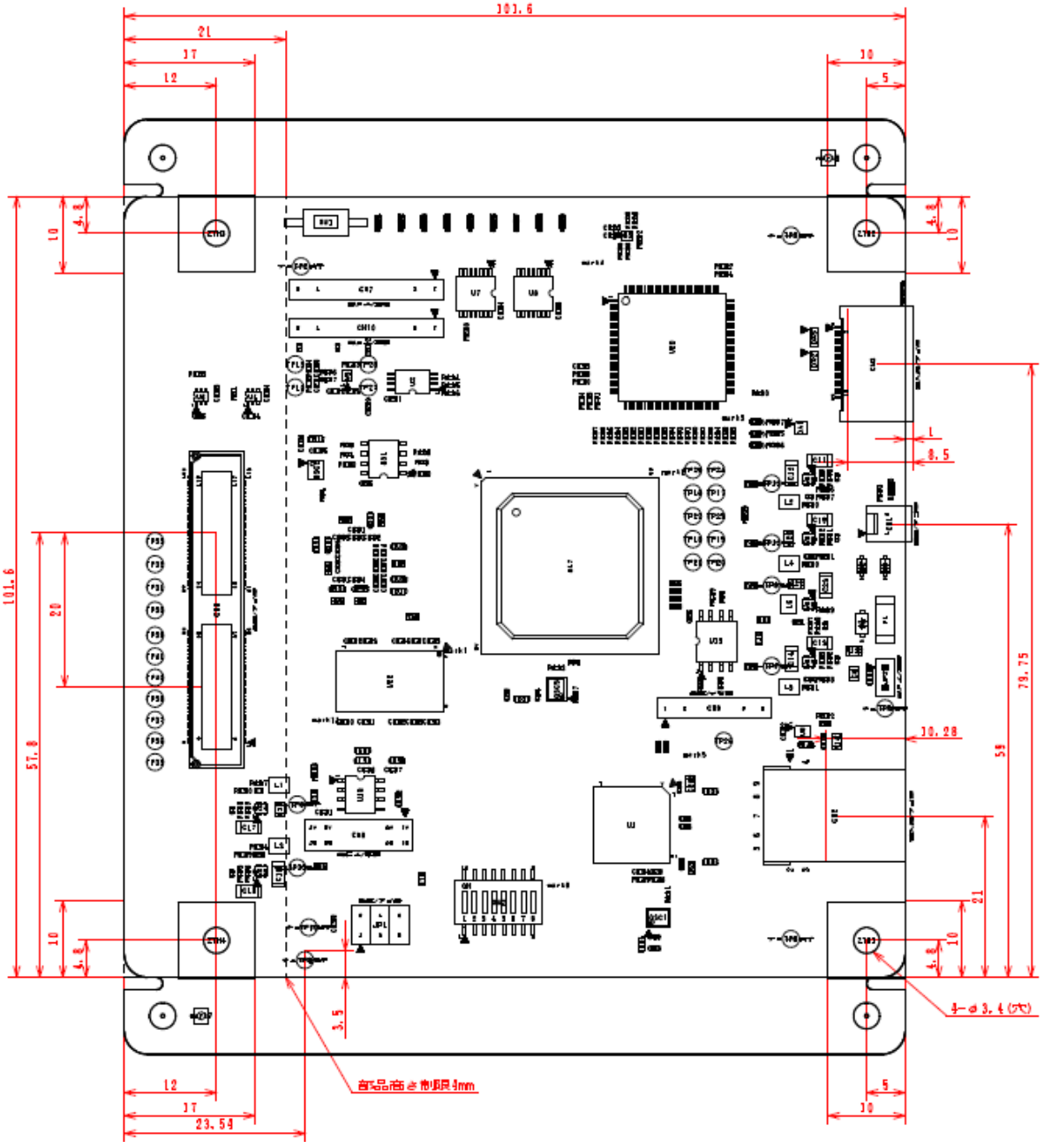
The SVM-06 Rev.1.4 board has been upgraded to enhance robustness compared to the Rev.1.3 board, without compromising the stability of USB communication or other operations. Despite the recent surge in manufacturing costs, the price remains unchanged from the Rev.1.3 board (domestic list price).

Some components have been modified or added for reasons of availability and cost optimization. Additionally, the solder mask color has been changed from black to green to improve PCB quality and ensure supply chain stability.

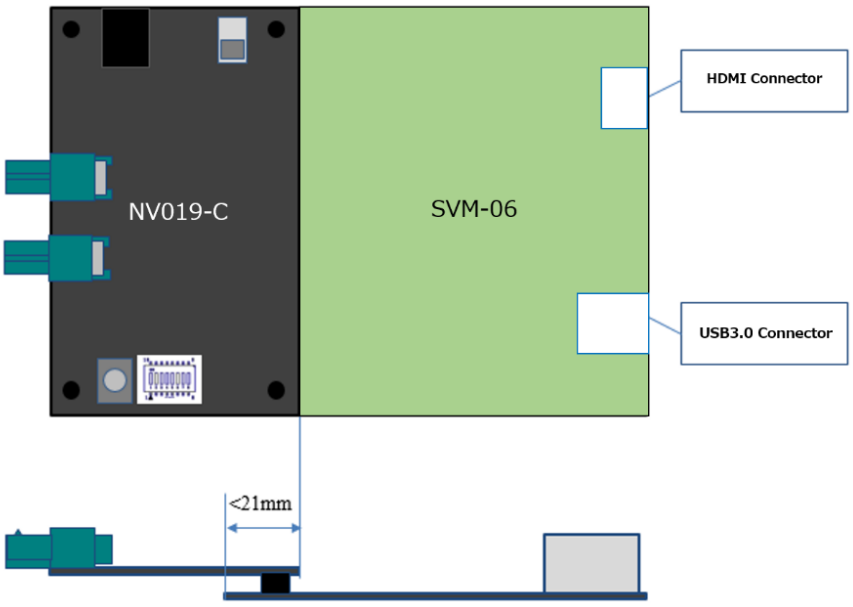
The connector layout and functionality remain unchanged from Rev.1.3, allowing the Rev.1.4 board to be used in the same way as the previous SVM-06 boards.

5.3. Drawing

The dimensions of the SVM-06 board are shown below. The actual board size does not include the 10mm VCUT parts at both the top and bottom edges. The external dimensions are 101.6 x 101.6 mm, which is the same as our other SV series boards.

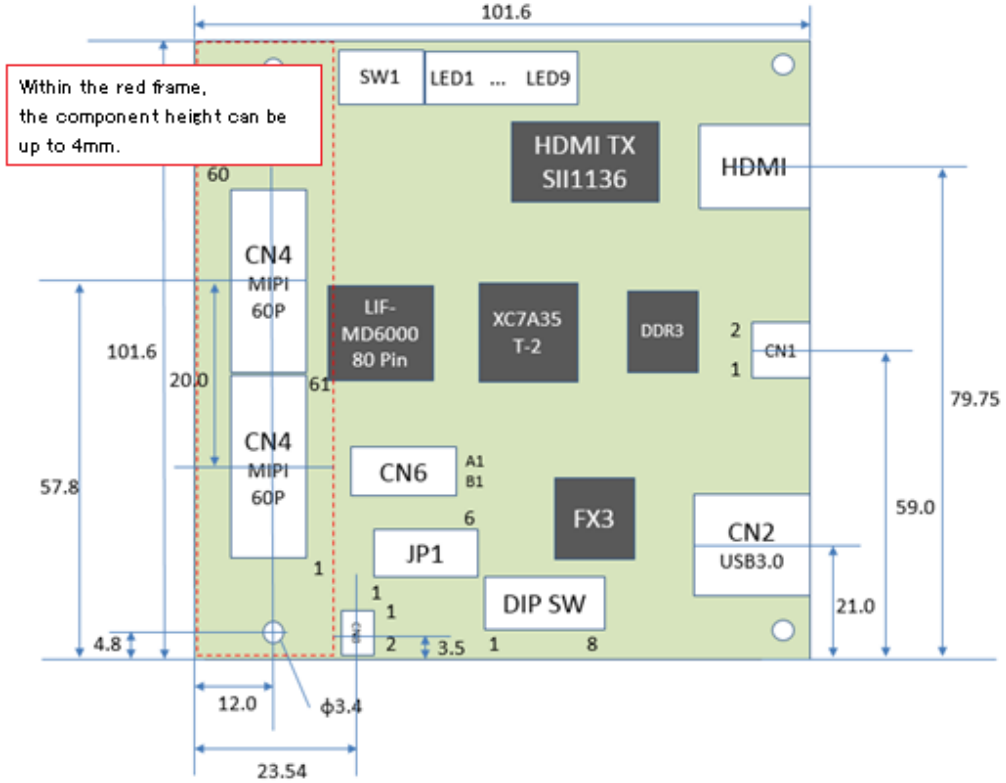


5.4. Dimensional Restriction of Connection Target Board



(Board connection example)

The SVM-06 board is used by connecting the target connection board to the connector CN4 as shown above. This connection board partially overlaps the SVM-06 board, but the overlapping area must not exceed 21mm from the edge of the SVM-06 board. This area is outlined by the red frame in the figure below. If using a connection board with dimensions that extend beyond this frame, ensure the board shape is compatible and use high connectors to allow proper connection of both boards.



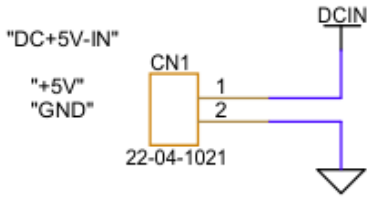
6. Connector Specification

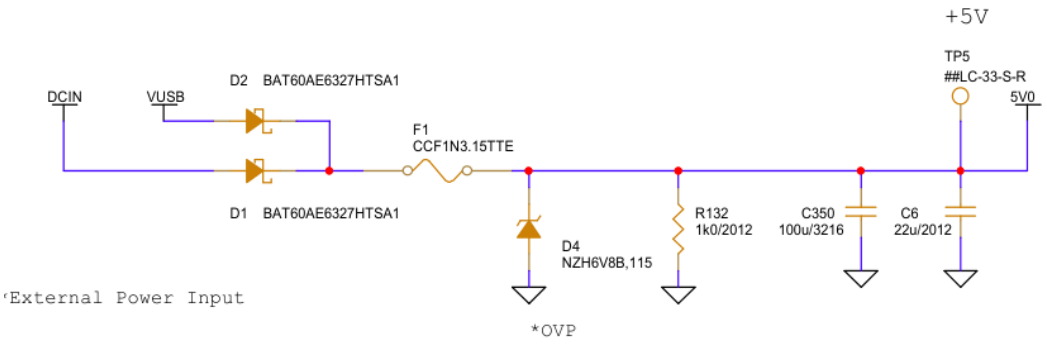
This chapter describes the specifications of the connector used to connect to the target. Other connectors are described in the Appendix.

6.1. CN1: Sub Power Connector

This is used when the USB bus power is insufficient or unavailable.

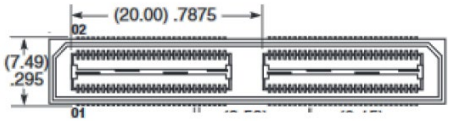
Connector		22-04-1021: Molex					
Pin #	Signal Name	Direction	Remarks	Pin #	Signal Name	Direction	Remarks
1	+5V	IN	DC5V power	2	GND	-	Power ground





- + 5V (DCIN) from CN1 and + 5V (VUSB) from the USB connector are connected via a diode OR as shown in the circuit diagram above. These serve as the internal 5V power supply for the board (5V0).

6.2. CN4: Target Connector



This connector is used to connect to the target device.

Main port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
61	D1_N	IN	MIPI Lane1 Input -	62	GPIO0	IO	GPIO 0 Trigger / FSYNC Input 1 (Reserved)
63	D1_P	IN	MIPI Lane1 Input +	64	GPIO1	IO	GPIO 1
65	GND	-		66	GND	-	
67	D3_N	IN	MIPI Lane3 Input -	68	GPIO2	IO	GPIO 2
69	D3_P	IN	MIPI Lane3 Input +	70	GPIO3	IO	GPIO 3 Trigger / FSYNC Output 1 (Reserved)
71	GND	-		72	GND	-	
73	CLK_N	IN	MIPI Clock Input -	74	GPIO4	IO	GPIO 4
75	CLK_P	IN	MIPI Clock Input +	76	GPIO5	IO	GPIO 5
77	GND	-		78	GND	-	
79	D2_N	IN	MIPI Lane2 Input -	80	GPIO6	IO	GPIO 6
81	D2_P	IN	MIPI Lane2 Input +	82	GPIO7	IO	GPIO 7
83	GND	-		84	GND	-	
85	D4_N	IN	MIPI Lane4 Input -	86	GPIO8	IO	GPIO 8
87	D4_P	IN	MIPI Lane4 Input +	88	GPIO9	IO	GPIO 9
89	GND	-		90	GND	-	
91	SCL	OUT	I2C SCL Signal Line	92	GPIO10	IO	GPIO 10
93	SDA	IO	I2C SDA Signal Line	94	GPIO11	IO	GPIO 11
95	GND	-		96	GND	-	
97	GND	-		98	NC	-	
99	GND	-		100	NC	-	
101	GND	-		102	GND	-	
103	VSYNC	IO	VSYNC IO (Reserved)	104	GPIO12	IO	GPIO 12
105	HSYNC	IO	HSYNC IO (Reserved)	106	GPIO13	IO	GPIO 13
107	GND	-		108	GND	-	
109	CK	OUT	Clock Output	110	GPIO14	IO	GPIO 14
111	RST	OUT	Reset Output (L : Reset)	112	GPIO15	IO	GPIO 15

113	GND	-		114	GND	-	
115	VDDIO	POW	IO Power Output	116	1V2	POW	1.2V Power Output
117	3V3	POW	3.3V Power Output	118	3V3	POW	3.3V Power Output
119	GND	-		120	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

Lane numbers are denoted as 1-4 instead of 0-3.

Extension port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	D1_N	IN	MIPI lane5 IO -	2	NC		Connected to TP35
3	D1_P	IN	MIPI lane5 IO +	4	NC		Connected to TP36
5	GND	-		6	GND	-	
7	D3_N	IN	MIPI lane7 IO -	8	NC		Connected to TP37
9	D3_P	IN	MIPI lane7 IO +	10	NC		Connected to TP38
11	GND	-		12	GND	-	
13	CLK_N	IN	MIPI clock 2 IO -	14	NC		
15	CLK_P	IN	MIPI clock 2 IO +	16	NC		
17	GND	-		18	GND	-	
19	D2_N	IN	MIPI lane6 IO -	20	NC		
21	D2_P	IN	MIPI lane6 IO +	22	NC		
23	GND	-		24	GND	-	
25	D4_N	IN	MIPI lane8 IO -	26	NC		
27	D4_P	IN	MIPI lane8 IO +	28	NC		
29	GND	-		30	GND	-	
31	SCL	OUT	I2C SCL Signal line	32	NC		
33	SDA	IO	I2C SDA Signal line	34	NC		
35	GND	-		36	GND	-	
37	NC	-		38	GND	-	
39	NC	-		40	GND	-	
41	GND	-		42	GND	-	

43	5V0	POW	+5V Power Output	44	NC		
45	5V0	POW	+5V Power Output	46	NC		
47	GND	-		48	GND	-	
49	NC			50	EXTIN14	IN	Tolerant input of GPIO14
51	NC			52	NC		
53	GND	-		54	GND	-	
55	VDDIO	POW	IO Power Output	56	5V0	POW	+5V Power Output
57	3V3	POW	3.3V Power Output	58	3V3	POW	3.3V Power Output
59	GND	-		60	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

- The connector position and pin assignment are upward compatible with the 60-pin connector from our previous boards. Therefore, interface boards designed for previous boards can be connected to the SVM-06.
- If the expansion port side (1-60P) is not used, it can be treated as a 60-pin connector (connection target: QTH-030-01-L-D-A). In this case, only the main port side (61-120P) should be used.
- The HSYNC and VSYNC pins are reserved for customization, and have no function in the standard version. (Hi-Z)
- GPIO pins are Hi-Z by default. The direction and level of each pin can be set via the FPGA registers.
- The IO voltages for each single-ended port are determined via jumper JP1.
- The clock output frequency is set using our software "SVMCtl".
- 1.2V, 3.3V and 5V can be output with max.150mA.
- SCL and SDA are connected to the I2C bus inside the SVM-06 via a level conversion IC.
- The EXTINn pin is 5V tolerant and is pulled down with 200kΩ resistor. Do not apply a voltage exceeding VDDIO to any other pins.
- EXTINn and GPIOn cannot be used simultaneously. When using EXTINn, the corresponding GPIOn pin must be left open. Similarly, when using GPIO14, the corresponding EXTINn must be left open.
- GPIO pins are controlled via FPGA registers. Please contact us for more details.

7. Component Details

7.1. SW1: Push Switch

SW1 is a switch used for outputting the reset signal or retransmitting the register initial settings. The function of SW1 can be selected via our software SVMCtl.

When SW1 is assigned to the reset output, the RST signal line assigned to CN4 is asserted (L output) while SW1 is pressed, and at the same time, the blocks inside the FPGA are also reset.

When SW1 is assigned to register initialization retransmission, the initialization file stored in the SPI-ROM on the board is retransmitted.

7.2. SW2: DIP Switch

SW2 is an 8-bit switch used for setting the various operating modes of SVM-06. You can set the following settings using this switch.

Number	Name	OFF	ON
1	HDMI Output Frame Rate (HDMI Mode Only)	60FPS	30FPS
2	Test Pattern Output	Normal mode	Test pattern output
3	MIPI lane count	3: OFF, 4: OFF -> 4 Lanes 3: ON, 4: OFF -> 1 Lane 3: OFF, 4: ON -> 2 Lanes 3: ON, 4: ON -> 3 Lanes	
4			
5	Monitor Output Resolution (HDMI Mode Only)	5: OFF, 6: OFF -> 1080p (1920 x 1080) 5: ON, 6: OFF -> 4k (Only 3840 x 2160, 30fps) 5: OFF, 6: ON -> 720p (1280 x 720) 5: ON, 6: ON -> (Custom Resolution) or 1440p (2560x1440)	
6			
7	Mode (When Power ON)	7: OFF, 8: OFF -> HDMI mode 7: ON, 8: OFF -> Updater mode 7: OFF, 8: ON -> UVC mode 7: ON, 8: ON -> (Reserved)	
8			

- In addition, some settings should be configured via SVMCtl.
- In HDMI mode, settings #1, #5 and #6 are valid only when timing data is not set via SVMCtl. If the timing data has been set, these switch settings are ignored.
- In HDMI mode, the default output format is RGB. It can be switched to YUV format using SVMCtl.
- For “Custom Resolution” of the monitor output resolution, when output timing data is set via SVMCtl, the resolution setting is applied. If output timing data is not set, 1440p resolution is output.

7.3. LED1-9: Operating Status Indicator

These LEDs display the operating status of the board or FPGA. During the startup process, they blink at high speed. After a successful startup, the LEDs operate as follows.

LED #	Description
1	Lights up to indicate that the power supply to CN4 is active.
2	Lights up to indicate that the clock supplied to the target is locked.
3	Lights up to indicate that the sync signal from the target has been successfully decoded and detected.
4	Toggles ON/OFF at a frequency of 1/3 the VSYNC period (FS/FE after MIPI decoding) from the target. For an input image at 30 fps, it blinks 5 times per second.
5	HDMI mode: <Reserved> UVC mode: Lights up when USB transfer cannot be completed on time causing frame drops due to buffer overflow. It is reset when "Preview" with our capture software (NVCap) is started.
6	<Reserved>
7	<Reserved>
8	Lights up during capture operations from the host PC via USB.
9	HDMI mode: Toggles ON/OFF at a frequency of 1/3 the VSYNC period of the HDMI monitor output. For an output image at 60 fps, it blinks 10 times per second. UVC mode: Toggles ON/OFF at a frequency of 1/3 the VSYNC period of the USB output.

- The LEDs labeled as <Reserved> above may be assigned functions in the future. In the current version, their lighting status varies depending on the internal stats.

7.4. JP1: VDDIO Selection Jumper

JP1 is a jumper for selecting the IO power supply (VDDIO) for the target device output from the SVM-06 the connector. It can be selected from 1.8 V, 2.5 V or 3.3 V.

VDDIO is intended to be used as an IO power supply voltage for the target devices. Additionally, the GPIO0-15, CLK, RST, SCL, and SDA signal lines operate at the VDDIO power supply level. By default, VDDIO is set to 3.3V.

7.5. JP3: Configuration Setting Jumper

JP3 is a jumper for configuration settings. It is typically left open (with no jumper pin connected) for normal use.

7.6. Operating Temperature Range

The operating temperature range of the ICs on the SVM-06 board is 0-80℃. However, this value does not

account for the heat generated by the devices themselves. To ensure the IC die operates within the 0-80°C range, the ambient temperature (operating temperature range) should be kept within 0-42°C in UVC mode and 0-36°C in HDMI mode. Although operation has been confirmed at temperatures up to 60°C, performance cannot be guaranteed at these temperatures.

When operating at temperatures exceeding the above ranges or when the board is enclosed in a case, it is recommended to attach a heat sink to the FPGA or use a cooling fan.

For reference, when a heat sink (LPD25-15B, 25x25x15mm) is attached to the FPGA and the board is naturally air-cooled in an open space, the upper limits of the operating temperature, calculated using the same method as above, are 55°C in UVC mode and 49°C in HDMI mode.
(Actual values measured by our company)

8. Check Terminal

8.1. TP4: VDDIO Check Terminal (Red)

TP4 is the test point used to check the VDDIO voltage.

8.2. TP1, 3, 5, 6: Voltage Check Terminal (Red)

These are the test points for each power supply voltage required for the operation of the SVM-06. Normally, there is no need to check these voltages. Additionally, do not use these check terminals to supply power to external modules.

8.3. TP7-10: GND Check Terminal (Black)

These are used as GND (ground) terminals.

9. Applicable Version

Mode	FX3 Version	FPGA Version
UVC mode	127 or later	1.70 or later
HDMI mode	126 or later	1.53 or later

- When using the SVM-06 rev.1.4, please use the latest version.

10. Notes

For proper use of the SVM-06, please be sure to follow the precautions below:

1. When updating the firmware / FPGA, set the DIP switch to #7 = ON, #8 = OFF and use our update software SVMUpdater on the host PC.
2. Before connecting or disconnecting the target, always turn off the power to SVM-06.
3. We do not guarantee image display on all HDMI monitors for each setting such as output resolution and frame rate. Supported specifications vary by monitor, and unsupported output formats may result in no display.
4. Please use a power supply with sufficient current capacity to supply power to the SVM-06 board.
5. The contents of this document are subject to change without notice.
6. Reprinting all or part of this document without permission is strictly prohibited.
7. If you find any errors or omissions, please contact us at: E-mail: sv-support@net-vision.co.jp
8. Be sure to use the latest version of SVMCtl / SVMUpdater software when purchasing the board. Using older software for updating or configuring the board may result in improper operation.
9. If the board power is turned on while the MIPI signal is already being input, the board may not start up properly. When turning on the board, ensure that signal transmission from the target device is stopped.
10. When inputting external signals into each signal line of connector CN4, ensure that the voltage does not exceed the VDDIO of the SVM-06. Do not input signals (including MIPI signals) when the SVM-06 is powered off, as this may cause malfunctions.
11. If the board is enclosed in a case, consider attaching a heat sink or cooling fan to ensure proper operation.

11. Appendix

11.1. CN2: USB3.0 Connector

This is the USB 3.0 connector for connecting to the host PC. A commercially available USB3.0 cable can be used. This connector also serves as the power supply for the SVM-06.

Connector		1003-024-02000					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	VBUS	IN	+5V Bus Power	2	D-	I/O	USB 2.0 Differential Pair -
3	D+	I/O	USB2.0 Differential Pair +	4	GND	-	GND for Power
5	SSTX-	OUT	USB3.0 Transmission Differential Pair -	6	SSTX+	OUT	USB 3.0 Transmission Differential Pair +
7	GND DRAIN	-	GND for Signal	8	SSRX-	IN	USB 3.0 Receiver Differential Pair -
9	SSRX+	IN	USB 3.0 Receiver Differential Pair +				

11.2. CN3: HDMI Connector

This is the HDMI connector for connection to the HDMI monitor or other device through an HDMI cable.

Connector		10029449-111RLF					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	D2+	OUT	TMDS Data 2 +	2	D2 shield	OUT	TMDS Data 2 shield
3	D2-	OUT	TMDS Data 2 -	4	D1+	OUT	TMDS Data 1 +
5	D1 shield	OUT	TMDS Data 1 shield	6	D1-	OUT	TMDS Data 1 -
7	D0+	OUT	TMDS Data 0 +	8	D0 shield	OUT	TMDS Data 0 shield
9	D0-	OUT	TMDS Data 0 -	10	CLK+	OUT	TMDS Clock +
11	CLK shield	OUT	TMDS Clock shield	12	CLK-	OUT	TMDS Clock -
13	CEC	I/O	CEC Data	14	Utility	IN	Utility
15	DDCSCL	(I)/O	DDC Clock	16	DDCSDA	I/O	DDC Data
17	GND	-	-	18	+5V	OUT	+ 5V Power
19	HPD	IN	Hot Plug Detection				

11.3. CN6: FPGA-JTAG Connector

This is a JTAG port used for writing the FPGA bitstream to the SPI-ROM or for debugging the running FPGA. This connector is not typically used.

Note: The direction is viewed from the FPGA.

Connector		A3B-14PA-2DSA(71)					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	GND	-		2	VREF	OUT	Reference Voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	(Disconnected)
13	GND	-		14	NC	-	(Disconnected)

- **We do not guarantee the operation when you use it.**