USB3.0 Video Capture Board

(SVP-01-UVC)

Hardware Specification

Rev. 1.2

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	30. Sep., 2022	New File (Translation of Japanese edition ver.1.3)	R.Sugo
1.1	16. Jan., 2025	Change the product name from “SVP-01-U” to “SVP-01-UVC”.	R.Sugo
1.2	18. Feb., 2025	Corrected the description of RGB888 in “SW2: DIP Switch” in chapter 6.3.	R.Sugo

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1. Outline

This document is a hardware specification of the **"SVP-01-UVC"**. SVP-01-UVC is a board for capturing video signals output from an image sensor with USB3.0 connection, and displaying on an external monitor with DisplayPort connection.

SVP-01-UVC has three modes; **UVC mode**, **DisplayPort mode** and **Updater mode**.

In UVC mode, you can capture video with PC as a UVC (USB Video Class) device that is the same as webcam, so you can evaluate image sensors and develop algorithms on various OS such as Windows and Linux. The board can operate on USB bus power. If the host PC does not have supply capacity enough, supply +5V from CN1.

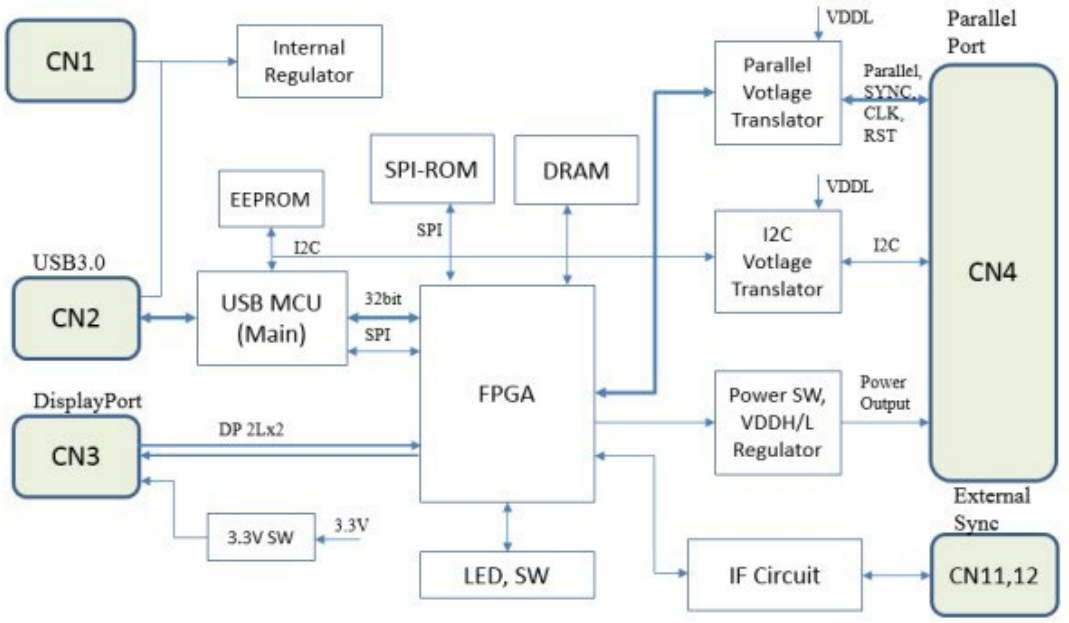
Video data is transferred to the PC via USB3.0, so this board supports uncompressed video data with a bandwidth of up to 3 Gbps. The device driver is unnecessary for video capturing, making it easy to connect to third party software such as OpenCV or ROS. (When changing the board setting, it is necessary to install the driver.)

In DisplayPort mode, you can display video on an external LCD monitor using a DisplayPort cable. Also using a DisplayPort - HDMI active converter cable, you can use a HDMI monitor.

In Updater mode, you can update the firmware of devices such as microcontroller and FPGA via USB. You cannot update in UVC mode, be sure to boot in Updater mode when updating.

You can switch each mode according to the startup state of #7 and #8 of the DIP Switch (SW2). This board operates in UVC mode when #7 = OFF and #8 = ON, in DisplayPort mode when #7 = OFF and #8 = OFF, and in Updater mode when #7 = ON, #8 = OFF.

1.1. Block Diagram



1.2. Specification

・Power : USB Bus Supply (External Power Supply can also be used)

-Supply voltage: +5V (4.75-5.5V)

-Operating current (typ): 0.72A (DisplayPort) / 0.6A (UVC)

・Input Format (Via CN4, 5):

-Parallel video signal (PCLK/VSYNC/HSYNC; Embedded Sync (BT.656) Supported.)

-PCLK < 150MHz

-Input Bit Width: 8bit / 16bit / 24bit / 32bit

-Input Pixel Format: YUV4:2:2 (8bit), RGB24, RAW

-IO Voltage (VDDL) Level: 1.8-3.3V

・Frame Memory: 256MB

-Only when the frame memory usage setting is enabled.

・Input Resolution: Up to 8190x4095 pixel (4094x4095 at 8bit)

-Input image can be clipped in any area.

・USB output: USB 3.0 (Operating in USB Video Class)

- Operating USB2.0 HS (480Mbps) is possible.

・DisplayPort output: DisplayPort 1.1a

- Raw Bit Rate = 2.7Gbps/Lane x 2L (Throughput 4.3Gbps)
- Dual-Mode (DP++): Incompatible
- DPCP: None

・Power output: IO voltage x1, Target voltage x2

・Serial communication: I2C (max. 400kHz, device address 7bit)

- IO voltage is the same as voltage level of video signal (VDDL).

・Reset signal output

・Clock signal output

・GPIO Input/Output (video signal + GPIO = Up to 32bit)

- By mounting connector CN5, 32bit can be used.

・USB device name

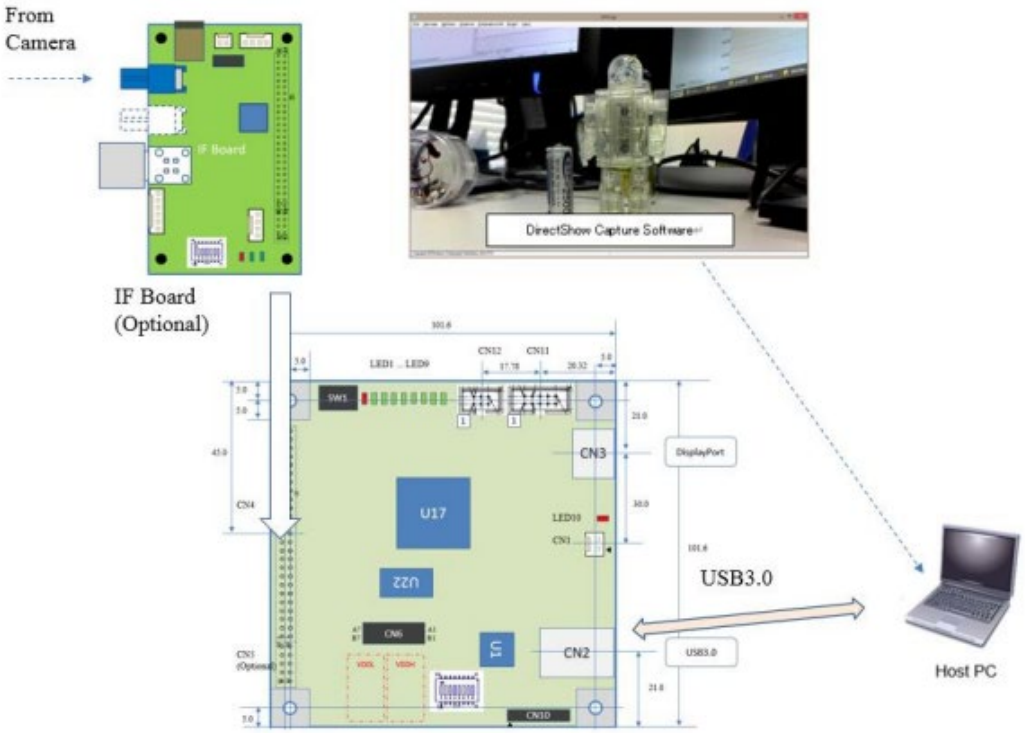
- UVC mode: “SVP-01-UVC”
- If you assign a board ID, a number such as "(1)" is added to the end of the board name.

2. UVC Mode Operation Details

This section describes **UVC mode** (parallel input / USB output).

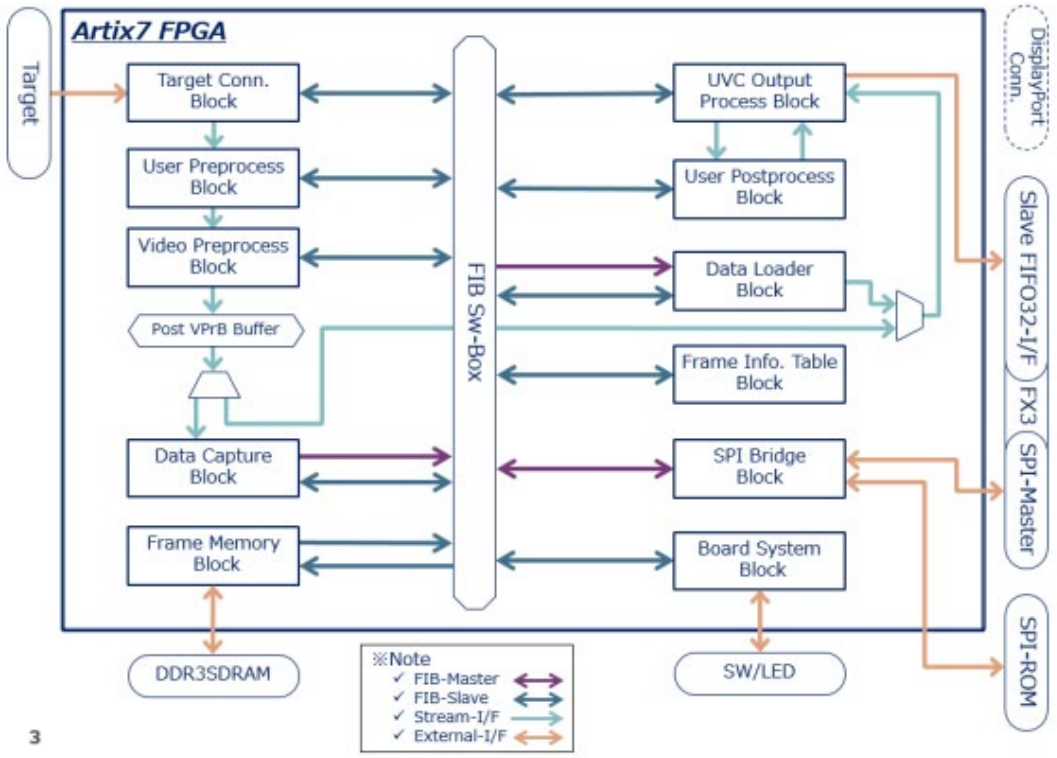
You can use UVC mode by booting this board with the DIP SW set to #7: OFF and #8: ON.

2.1. UVC Mode Connection Configuration Example



- USB connector supplies power to this board.
- If the host PC does not have supply capacity enough, supply +5V from CN1.

2.2. FPGA Internal Block Diagram in UVC Mode



2.3. Format Setting

In UVC mode, you need to set resolution, frame rate, output pixel format setting, and sync signal setting. These settings are written via USB connector with SVMCtl. Once you have done the initial setting, you do not need to set it after that.

Set the resolution and frame rate according to the input video. If you want to output only a part of the input image, set the clipping settings. In this case, set the resolution after clipping.

For parallel video signals, the polarity of the synchronization signal must be set appropriately. You can set the polarity of VSYNC, HSYNC, DE (when used) arbitrarily. Also, if you input the signal of BT.656 format Embedded Sync, enable embedded synchronization.

The output pixel format is set according to the input pixel format of the video signal. You can set UYVY, YUY2, and RGB24 with SVMCtl, among the uncompressed video pixel formats supported as standard by many OSs. For RAW format, it can be set as UYVY or YUY2 format and displayed in grayscale or color with the display plug-in of the capture software (NVCap). If you need to use other output pixel formats, basically customization is required, so please contact us.

The bus width of the input signals is set from 8bit - 32bit with DIP SW setting. For RGB24 input, 24 bit/pixel is supported.

2.4. Automatic Frame Rate Adjustment According to USB Transfer Bandwidth

The USB3.0 transfer bandwidth (theoretical value) is up to 3 Gbps, and the USB2.0 HS transfer bandwidth is 480 Mbps, but the input signal band supports higher data rates. Also, the actual usable USB bandwidth depends on the host controller and environment.

By enabling the automatic frame rate adjustment function, the output frame rate is automatically adjusted to match the effective USB bandwidth, and it is possible to capture video signal input in throughput that exceeds the USB bandwidth. You can this function by selecting the "Decimation" setting to "Auto" with SVMCtl and rebooting the board, and it must be enabled when the video signal input which peak bandwidth exceeds the USB bandwidth. Enabling it, the frame memory also enables and increases the latency of data.

If the USB output is not completed in time and the frame memory is full, the newly input frames are discarded.

2.5. Procedure of the UVC Mode Setting

As mentioned above, UVC mode requires initial setting according to the specifications of the image sensor at first use. If the setting is different from the output of the image sensor, it cannot be captured normally.

1. Setting of the target side power supply voltage (VDDH, VDDL)

Before connecting the target device, you must match the VDDL to the IO voltage of the target device. The VDDH voltage is the power supply voltage supplied to the target device, so set it according to the requirements of the device.

VDDL/VDDH can be switched by VR on the board. It is set to 3.3V at the time of shipment.

2. Setting of the DIP SW

It is necessary to set the DIP SW according to the bit width of the target device. See "SW2: DIP Switch" for the setting. It is set to 8bit at the time of shipment.

3. Initial setting with PC

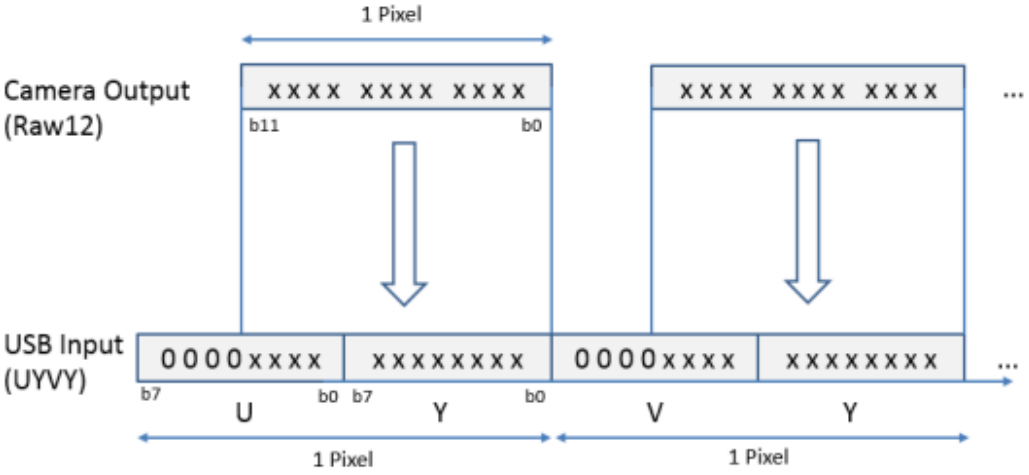
It is necessary to make initial settings such as resolution and pixel format with PC. You can set it with “SVMCtl” software. Refer to the “SVMCtl software manual” for how to use SVMCtl.

- SVMCtl may be updated from time to time. You can download the latest version from our web page.
- SVMCtl can only support Windows (after Windows7) environment.
- This board is recognized capture device with the name SVP-01-UVC by the PC.
- If you assign a device number with SVMCtl, the ID number is added after the device name.

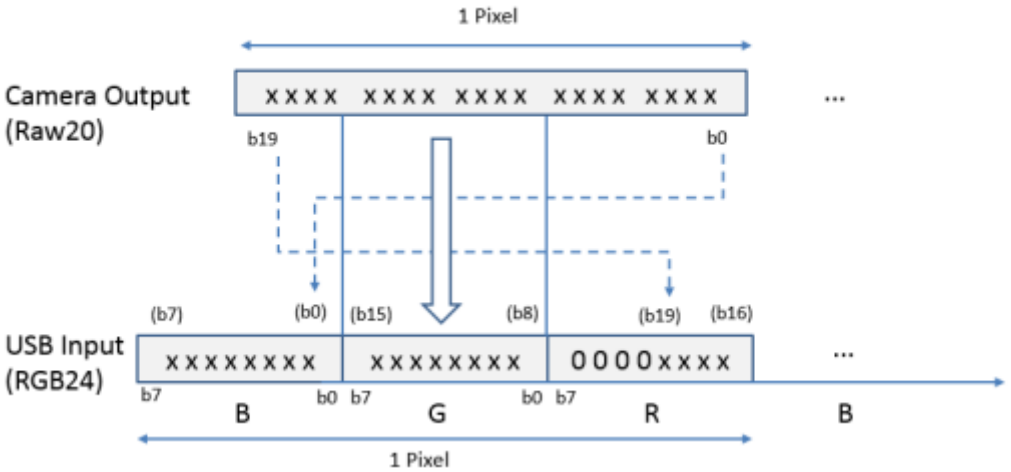
2.6. Processing at RAW Input

For RAW output image sensors, the UVC mode supports RAW8 / RAW10 / RAW12 / RAW16 / RAW20 formats. The UVC standard does not support the Raw format. For RAW8 – RAW12, the input data is captured in 16bit width and output to PC. Unconnected bit are indeterminate values, so it is recommended to use an external pull-down or pull-up.

When capturing RAW format, you need to specify UYVY in the pixel format setting to import the data that is packed to 16bit/pixel, and process the raw image using software on the host PC. In addition, you can set the RAW input to monochrome YUV 8bit format with SVMCtl and output it.



For RAW20, the input data is assumed to be 24bit width and output to the PC. Specify RGB24 in the pixel format setting to pack the image into 24 bit/pixel, and then process the RAW image using the host PC's software.



※On the host side, it is treated as RGB24, and the upper bit are padded with 0.

(Bitrate is 6/5 times)

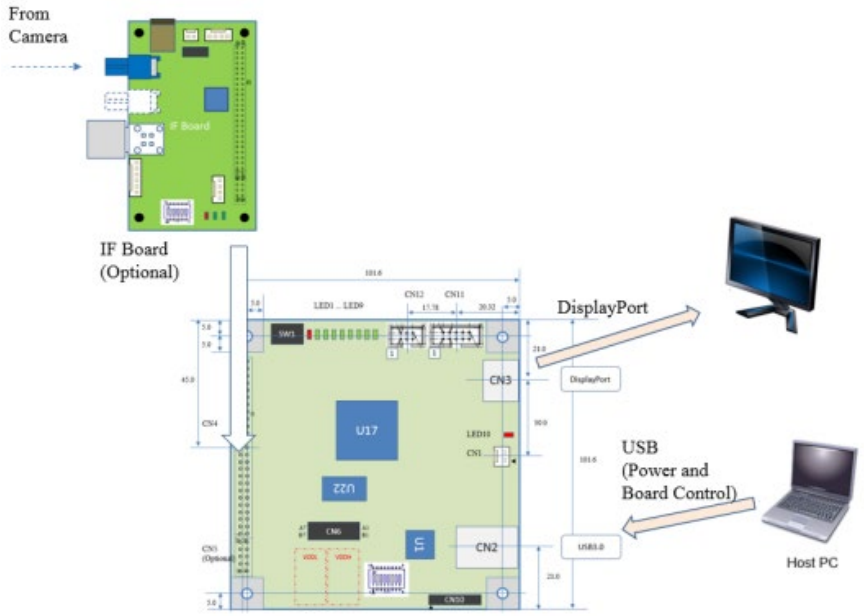
For board settings at the Raw input, also see "SVMCtl Software Manual".

3. DisplayPort Mode Operation Details

This section describes DisplayPort mode (parallel input / DP output).

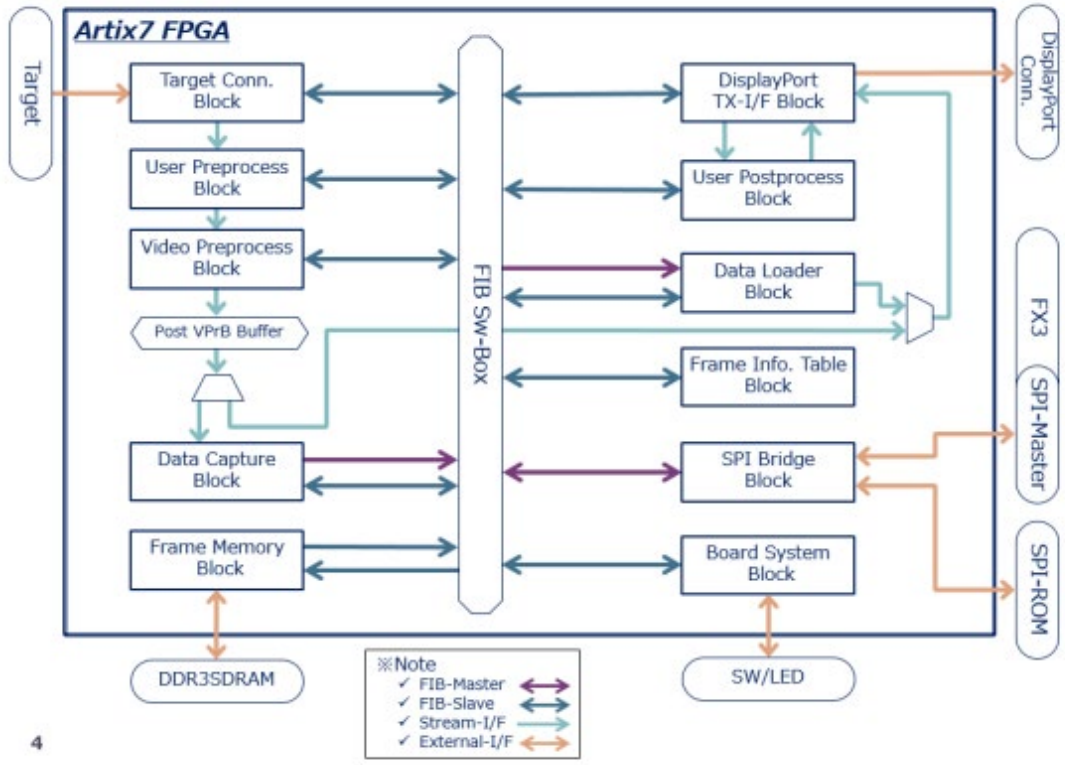
You can use DisplayPort mode by booting this board with the DIP SW set to #7: OFF and #8: OFF.

3.1. Connection Configuration Example of DisplayPort Mode



- For Initial board settings, I2C setting and power supply, the USB connector is used.
- This board can operate with supplied +5V from CN1. In this case, you do not need to connect the USB connector.
- DisplayPort output and USB output cannot be used at the same time.

3.2. FPGA Internal Block Diagram in DisplayPort Mode



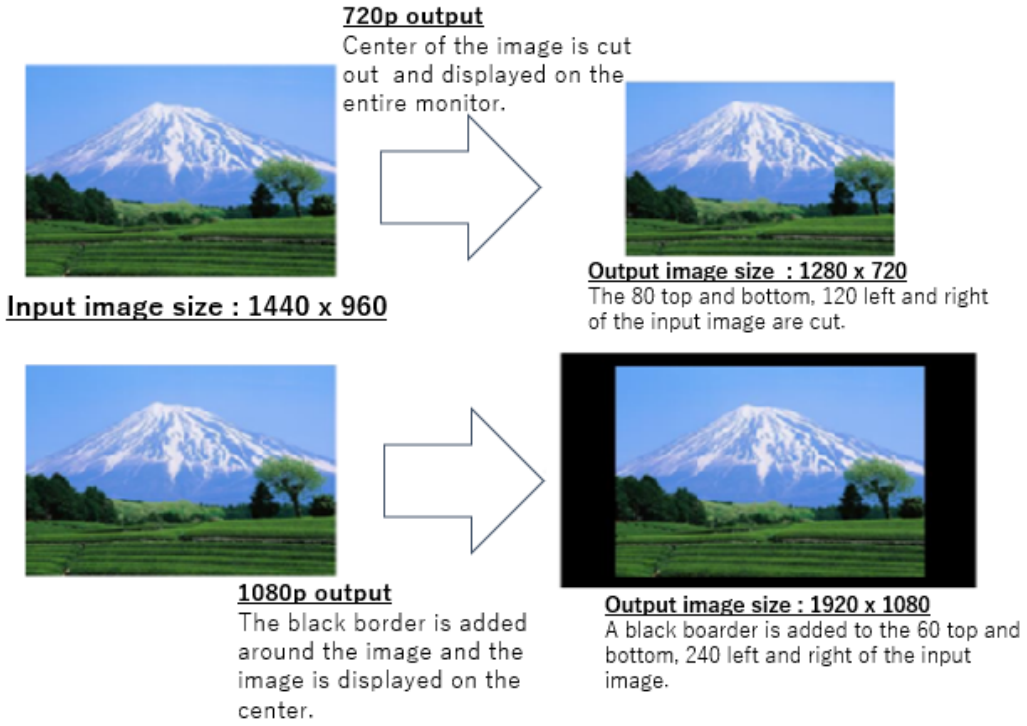
3.3. Format Setting

In DisplayPort mode, you need to set resolution, frame rate, output pixel format setting, and sync signal setting. These settings are written via the USB connector with SVMCtl. Once you have done the initial setting, you do not need to set it after that.

Set the resolution and frame rate according to the input video. If you want to output only a part of the input image, set the clipping settings. In this case, set the resolution after clipping.

This board does not have a scaling function. If the input resolution is smaller than the output one, add a black border around it. If the input resolution is larger than the output one, it is clipped in the center. You can also specify the cutout position with the clipping function.

For parallel video signals, the polarity of the synchronization signal must be set appropriately. You can arbitrarily set the polarity of VSYNC, HSYNC, DE (when used) arbitrarily. Also, if you input the signal of BT.656 format Embedded Sync, enable embedded synchronization.



You can specify the bus width from 8bit-32bit. If you use RGB24 input, set it to 24bit/pixel.

3.4. Raw Input Processing

When inputting a Raw image sensor signal, there is no Bayer -> Color conversion function in the DisplayPort mode. However, you can output image as a monochrome one in 1 pixel (dot-by-dot) per pixel. At this time, only the upper 8 bits are output, so if signals with a bit width of RAW10 or more is input, the lower bits are truncated.

If you want to output image as monochrome one, you need to set the Bit Shift and the Raw Processing on the SPI-ROM of the board with “SVMCtl”. If you don’t do these settings, the input will be processed as YUV and will not be displayed correctly.

3.5. Custom Resolution

You can select an output resolution (custom resolution) other than 1920 x 1080 / 1280 x 720 by turning on the DIP switch #4. When outputting an image at a custom resolution, you can specify the timing of the output video signals in pixel clock units. By writing the timing data with SVMCtl to the SPI-ROM on the board, it can operate as arbitrary timing output mode. The custom resolution output is unavailable if timing data is not written to SPI-ROM.

We do not yet have a document about how to create the timing data. If you want to use it, please contact us and inform the output resolution, frame rate and pixel clock.

4. Shape of the SVP-01-UVC Board

The photo and diagram of this board are shown below.

4.1. Photo of the Board

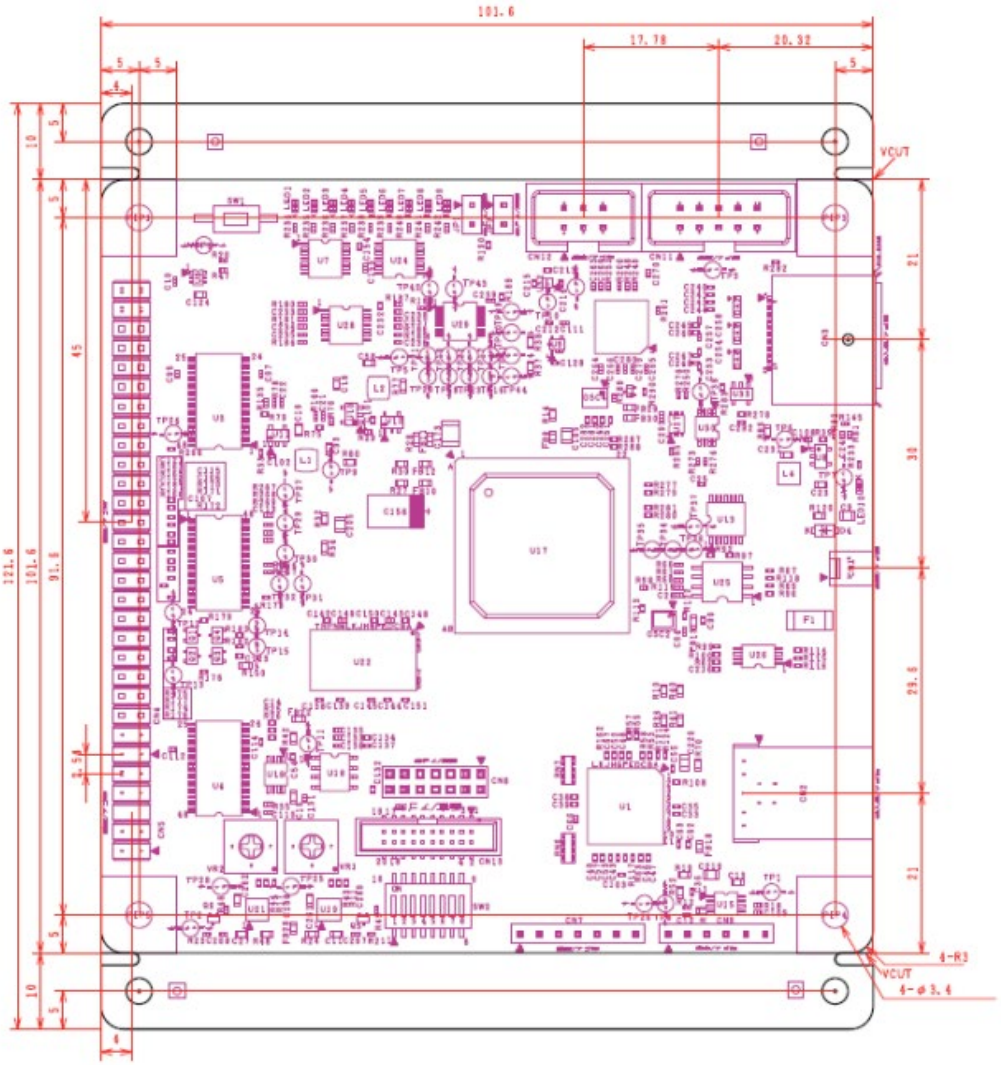
- Depending on the lot, the mounting state of the parts may be different.

- SVP-01-UVC, SVP-01-GEN and SVP-01-VND are using same board, but the firmware is different.

Refer to the label on the back of the board for the board type.

4.2. Drawing

The top and bottom 10mm are discarded plates. It does not attach the board.



5. Connector Specification

This chapter describes the connector specifications that should be considered when connecting to a camera or during normal use.

5.1. Connector List

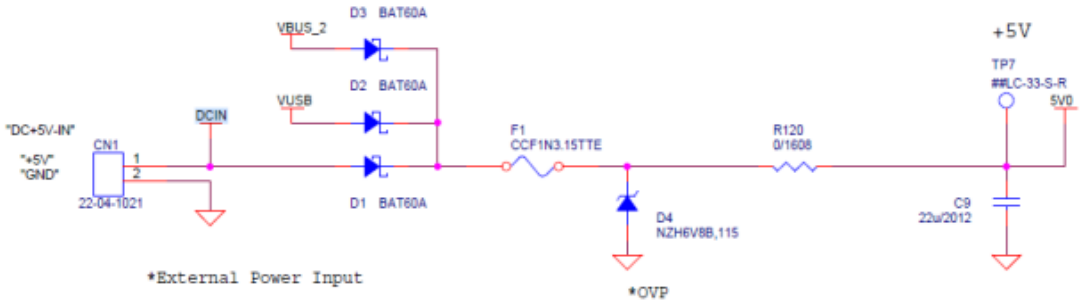
CN#	Mounted State	Model number	Function
CN1		22-04-1021	Sub power connector
CN2		1003-024-02000	USB3.0 type-B connector
CN3		0472720001	DisplayPort connector
CN4		PRPC025DAAN-RC	Parallel signal input/output (1-50P)
CN5	Un-mounted	PRPC005DAAN-RC	Parallel signal input/output (51-60P)
CN6		0877581416	JTAG connector
CN7	Un-mounted	A2-7PA-2.54DSA	(For debug)
CN9	Un-mounted	A2-6PA-2.54DSA	(For debug)
CN10	Un-mounted	A2-6PA-2.54DSA	(For debug)
CN11	Un-mounted	87834-1019	For synchronous wiring connector (5x2)
CN12	Un-mounted	87834-0619	For synchronous wiring connector (3x2)
CN13		3220-20-0300-00	For shipping check connector

- The mounted State is standard specifications of SVP-01-UVC.
- CN6-CN13 don't use normally.
- CN5 is used when expand the bit width of the parallel signals.

5.2. CN1: Sub Power Connector

This power connector is used when the USB bus power cannot meet the power capacity.

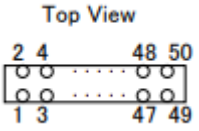
Used connector		22-04-1021: Molex					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
1	+5V	IN	DC5V power input	2	GND	-	Power ground



- The power input of CN1, the VBUS (VUSB) of CN2, and the VBUS (VBUS_2) of CN3 are connected by diode OR as shown in the above figure.
- Input voltage range is 4.75 - 5.5V.

5.3. CN4: Target Connection Connector A

This connector connects to the target image sensor, and is a pin header with a pitch of 2.54mm. It can be connected using a general pin socket or IDC cable. By using CN4 and CN5 in combination, you can connect an image sensor with a bit width of 24-32 bits.

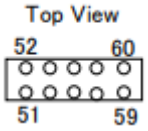


Using connector		PRPC025DAAN-RC					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
1	VDDL	OUT	IO voltage level output (1.8-3.3V)	2	GND	-	-
3	P0	IN	General purpose input port 0/ Pixel_DATA16	4	GND	-	-
5	P1	IN	General purpose input port 1/ DE input (8-16bit)/Pixel_DATA17	6	GND	-	-
7	P2	IN	General purpose input port 2/ Pixel_DATA18	8	GND	-	-
9	P3	OUT/IN	General purpose output port 0/ Pixel_DATA24	10	GND	-	-
11	P4	OUT/IN	General purpose output port 1/DE input (24bit)/ Pixel_DATA25	12	HSYNC	IN	Horizontal synchronization input
13	VSYNC	IN	Vertical synchronization input	14	XRST	OUT	Reset signal output
15	VDDH	OUT	Target power output (1.2 - 3.6V can be set)	16	GND	-	-
17	SDA	IO	I2C_DATA	18	GND	-	-
Using connector		PRPC025DAAN-RC					

Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
19	SCL	IO	I2C_CLK	20	GND	-	-
21	DCK	IN	Pixel_CLK (Pixel clock input)	22	GND	-	-
23	Y0	IN	Pixel_DATA0	24	GND	-	-
25	Y1	IN	Pixel_DATA1	26	GND	-	-
27	Y2	IN	Pixel_DATA2	28	GND	-	-
29	Y3	IN	Pixel_DATA3	30	GND	-	-
31	Y4	IN	Pixel_DATA4	32	GND	-	-
33	Y5	IN	Pixel_DATA5	34	GND	-	-
35	Y6	IN	Pixel_DATA6	36	GND	-	-
37	Y7	IN	Pixel_DATA7	38	GND	-	-
39	CLKOUT	OUT	Target drive clock	40	GND	-	-
41	Y8	IN	Pixel_DATA8	42	Y9	IN	Pixel_DATA9
43	Y10	IN	Pixel_DATA10	44	Y11	IN	Pixel_DATA11
45	Y12	IN	Pixel_DATA12	46	Y13	IN	Pixel_DATA13
47	Y14	IN	Pixel_DATA14	48	Y15	IN	Pixel_DATA15
49	3V3	OUT	3.3V Output	50	P5	OUT/IN	General purpose output port 2/ Pixel_DATA26

5.4. CN5: Target Connection Connector B

This connector connects to the target.

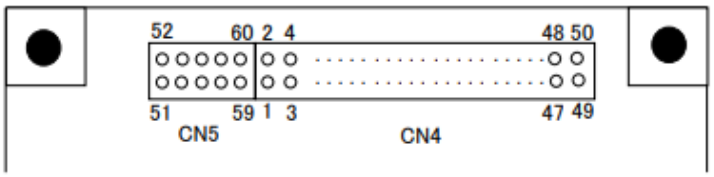


Using connector		PRPC005DAAN-RC					
Pin number	Signal name	Direction	Note	Pin number	Signal name	Direction	Note
51	P6	OUT/IN	General purpose output port 3/ Pixel_DATA27	52	P7	OUT/IN	General purpose output port 4/ Pixel_DATA28
53	P8	OUT/IN	General purpose output port 5/ Pixel_DATA29	54	P9	OUT/IN	General purpose output port 6/ Pixel_DATA30
55	P10	OUT/IN	General purpose output port 7/ Pixel_DATA31	56	P11	IN	General purpose input port 3/ Pixel_DATA19
57	P12	IN	General purpose input port 4/ Pixel_DATA20	58	P13	IN	General purpose input port 5/ Pixel_DATA21
59	P14	IN	General purpose input port 6/ Pixel_DATA22	60	P15	IN	General purpose input port 7/ Pixel_DATA23

-CN5 is optional. The Pin header is not mounted on SVP-01-UVC standard version.

-The input/output direction of Pixel_DATA [31:24] is changed depending on input bit width setting.

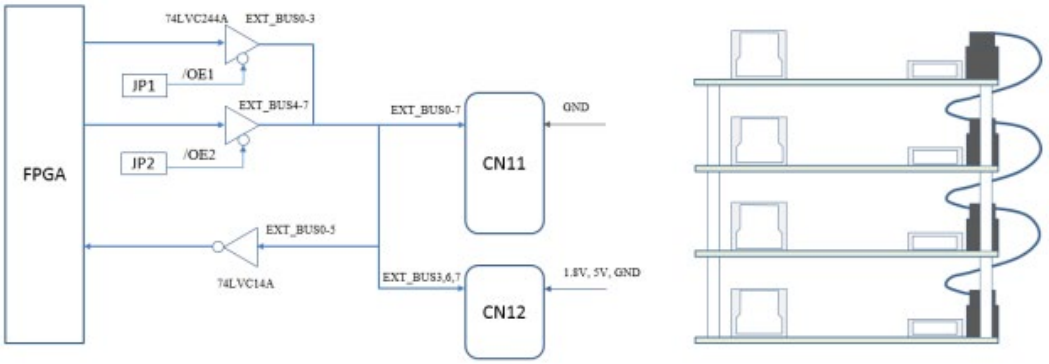
5.5. Positional Relationship Between CN4 and CN5



- You can use CN4 and CN5 as a 60pin pin header in combination.

5.6. CN11, CN12: Connector for Synchronous Wiring

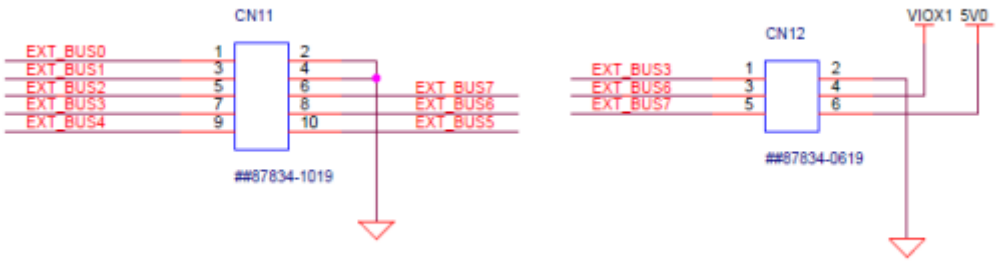
The CN11, CN12 are connectors for synchronous wiring between board to board. You can wire by using 2.54mm pitch IDC connector. You can use custom functions such as synchronous capturing and time stamping by connecting multiple SV series boards. This connector does not used in the standard specification. (It will be supported in the future.)



(Block Diagram)

When the JP1 is shorted, the EXT_BUS0-3 signal line becomes output. When JP2 is shorted, the EXT_BUS4-7 signal line becomes output.

(Pin Assignment)



5.7. Configuration Table of Input Data

When you use a YUV sensor or a RGB24 sensor, connect the wires according to the table below.

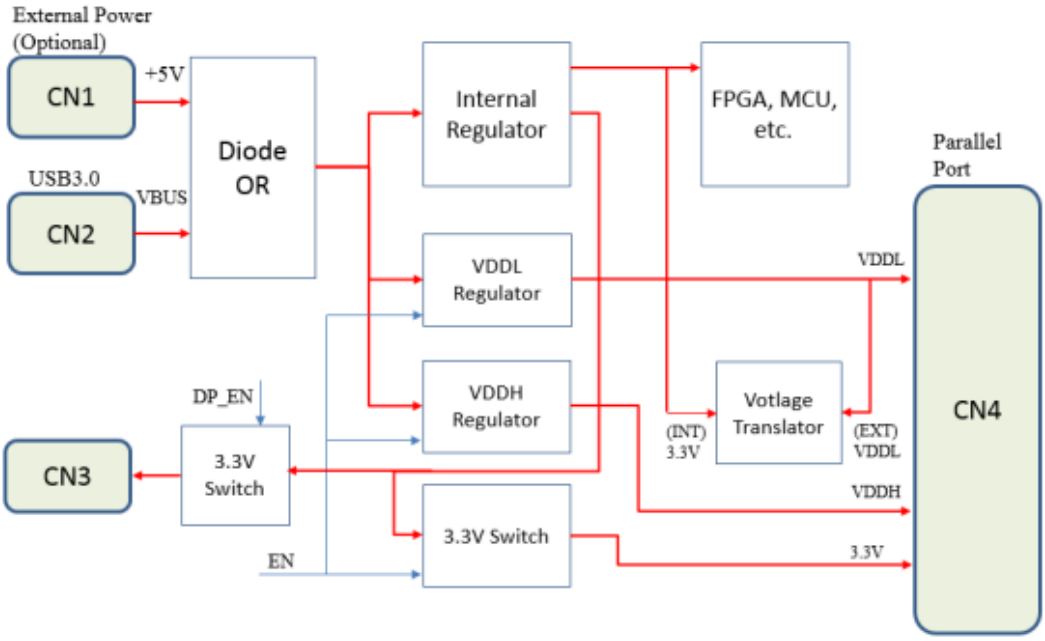
Format	YUV4:2:2			RGB24
Bit Width	8bit (UYVY/YUY2)	16bit (UYVY)	32bit (UYVY)	24bit
Pixel_DATA [31:24]	-	-	V	-
Pixel_DATA [23:16]	-	-	Y	R
Pixel_DATA [15:8]	-	U, V	U	B
Pixel_DATA [7:0]	Y, U, V	Y	Y	G

-The polarity of the VS, HS, and clock signals can be set arbitrarily.

6. Details of Each Part

6.1. Power Supply System

The power supply system of this board shown below. The board power supply can be operated by USB power supply or external +5V. Some of the internal regulator outputs are connected to CN4, and the connected device can also operate with USB power supply.



6.2. SW1: Push Switch

SW1 is a switch for functions such as controlling the reset output signal line and sending the initial settings to the I2C bus. You can change SW1 function with SVMCtl. You can check the SVMCtl software manual for more information.

6.3. SW2: DIP Switch

This is an 8bit switch for setting various operating modes. You can set the following items depending on the mode.

6.3.1. UVC Mode

No.#	Project	OFF	ON
1	Camera input bit width setting 1 (Only when #3=OFF)	8bit x 2 CLK	16bit x 1 CLK (YUV) or 24bit x 1 CLK (RGB)
2	Test pattern output	Standard operation	Test pattern output
3	Camera input bit width setting 2	(Following #1)	32bit x 1/2 CLK
4	-	-	-
5	-	-	-
6	-	-	-
7	Operation mode setting (When start up)	7:ON, 8:OFF: Updater mode 7:OFF, 8:ON: UVC mode 7:OFF, 8:OFF: DisplayPort mode 7:ON, 8:ON: Reserved	
8			

#4 and #6 are reserved for future functions. Normally, these switches should be set to OFF.

6.3.2 DisplayPort Mode

No.#	Project	OFF	ON
1	Camera input bit width setting 1 (#3=OFF)	8bit x 2 CLK	16bit x 1 CLK (YUV) or 24bit x 1 CLK (RGB)
2	Test pattern output	Standard operation	Test pattern output
3	Camera input bit width setting 2	(Following #1)	32bit x 1/2 CLK
4	Select custom resolution	Standard operation (Resolution specified by #5,6)	Custom resolution output (Resolution specified in SVMCtl)
5	Monitor output format setting	ON: RGB888 Output OFF: YUV422 8-bit Output	
6	Monitor output resolution setting	ON: 720p (1280x720) OFF: 1080p(1920x1080)	
7	Operation mode setting	7:ON, 8:OFF: Updater mode	

8	(When start up)	7:OFF, 8:ON: UVC mode 7:OFF, 8:OFF: DisplayPort mode 7:ON, 8:ON: Reserved

- When "The monitor output format setting" is ON, the video data is converted to RGB format and output to DisplayPort. When it is OFF, video data is output to DisplayPort in YUV format.
- The default frame rate for DisplayPort output is 60fps. However, if the custom resolution settings are not written to the board, setting #4 = ON will result in 30fps output.
- #5 = OFF (YUV422 output) may not be supported with all monitors. If your monitor does not support it, change it to RGB888 and output it, but the color will not be reproduced correctly. If there is no video on the monitor, set #5 = ON (RGB output).

6.4. **LED1-10**: Display the Operating Status

The LEDs display the operating status of such as board and FPGA.

LED#	Explanation
1	When the power is being supplied to the target, light up. This is a red LED.
2	When the clock supplied to the target is locked, light up.
3	When the synchronization signal for video input from the target is detected, light up.
4	This light turns ON/OFF at the cycle of the VSYNC synchronization signal from the target divided by 3. If the input image is 30 fps, it repeats flashing 5 times per second.
5	(DisplayPort mode) <Reserved> (UVC mode) When a frame drop occurs due to a delay in USB transfer and a buffer overflow, light up. You can reset it by starting a preview in capture software (NVCap).
6	<Reserved>
7	<Reserved>
8	(DisplayPort mode) <Reserved> (UVC mode) When this board captures video from the host PC, light up.
9	(DisplayPort mode) This light turns ON/OFF at the cycle of the VSYNC synchronization signal to the DisplayPort monitor output divided by 3. If the output image is 60 fps, it repeats flashing 10 times per second.

	(UVC mode) This light flash at a cycle by dividing the FV (Frame Valid) pulse of the UVC output from the Main port by 3.
10	When the power is being supply to the board, light up. This is a red LED.

- LEDs marked as Reserved in the table will be assigned for future function. In the current version, these LEDs change their lighting state depending on the state inside the board.
- When the I2C setting is being sent, the LED1-8 flash at high speed.
- If the license key has not been written to the board, LED1-8 will light up in order at low speed.
- During the DisplayPort connection process in the DisplayPort mode, LED1-6 are light up in order depending on the state. After the connection process is complete, it will be returned to the original state.
- If the board stops due to USB error, all LED will flash at low speed at the same time.

6.5. **VR1, VR2**: Connectors for Adjusting VDDH and VDDL

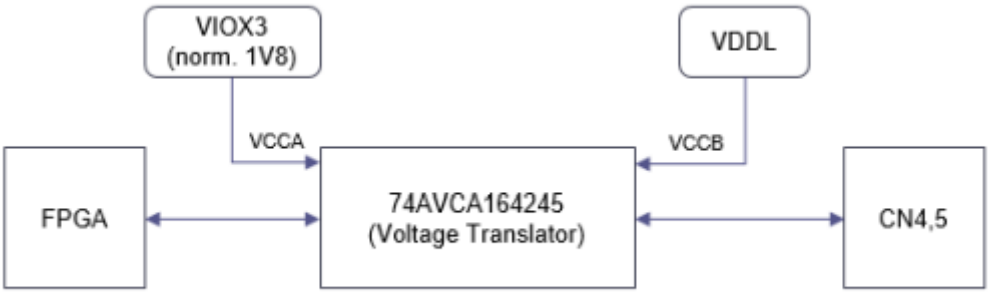
These are variable resistors for adjusting the power supply for the target device generated by SVP-01-UVC. VDDL can be adjusted in the range of 1.8V-3.3V and VDDH in the range of 1.2-3.6V.

The VDDL is connected to the translator IC, and the voltage level of the parallel video input signal and general input / output are the VDDL voltage. The VDDL must be set according to the target.

On the other hand, the VDDH output to only the connector and is not used inside the board. It can be used as the power supply for the target.

The VDDL and VDDH are set to 3.3 V at the time of shipment. You should adjust them according to the target side before use.

6.6. CN4,5 Input/Output Circuit Schematic Diagram



-The IO voltage of each single ended IO pin on CN4, CN5 side is determined by the VDDL voltage.

6.7. The Operating Temperature

The operating temperature range of the ICs on this board is 0-80℃. However, this value is not considered about the heat generation of the device.

Therefore, when the device is operating, the ambient temperature (the operating temperature range) should be 0-42°C in UVC mode and 0-36°C in DisplayPort mode. We have confirmed that it works even at temperatures higher than this (60°C), but we cannot guarantee it.

If you want to operate it in a higher temperature or if you put it into a case, it is recommended to attach a suitable heat sink to the FPGA or cool it with a fan.

For reference, if the heat sink LPD25-15B (25x25x15mm) is attached to the FPGA and cools in an open space, the upper operating temperature limit calculated in the same way is 55°C in UVC mode and 49°C in DisplayPort mode. (Measured by our company)

7. Applicable Version

This document supports the following versions.

Mode	FX3 Version	FPGA Version
Updater mode	After 101	After 0.20
UVC mode	After 116	After 1.03
DisplayPort mode	After 116	After 1.03
SVMCtl	After v1.4.7.2	
SVMUpdater	After v1.7.3.0	

8. Precaution

When using this board, please observe the following precautions.

1. When updating the farm / FPGA, set the DIP SW (SW2) #7 = ON, #8 = OFF and use update software (SVMUpdater) on the host PC.

2. When you connect and disconnect the target such as interface board, please turn off the SVP-01-UVC.

3. When you connect a device to the interface board or DisplayPort, the current consumption is also required. Therefore, please use a power supply that has sufficient power supply and current capacity for this board.

4. The contents of this document may change without advance notice.

5. We have made every effort to ensure that the contents of this document are complete, but if you notice any suspicious points, errors, omissions, etc., please contact to sv-support@net-vision.co.jp.

6. Be sure to use the SVMCtl / SVMUpdater software released after the development of SVP-01-UVC (SVMCtl is after v1.4.7.2, SVMUpdater is after v1.7.3.0). If you update or setting this board using an older version of the software, the software may not recognize the SVP-01-UVC and may not work properly.