

MIPI Generator
[SVL-03-GEN rev.1.2]
Hardware Specification

Ver.1.0

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	25. Feb., 2026	New File (Translated from Japanese version 1.0)	R. Sugo

Index

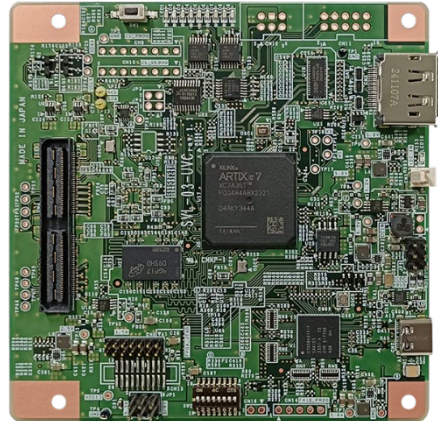
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1. Overview

This document describes the hardware specifications for the “SVL-03-GEN”, which converts video input from a PC via USB or DisplayPort into a MIPI CSI-2 standard video signal. This board is developed as the successor to our generator “SVO-03-MIPI”.

The operating mode of this board is specified by the on-board [SW2 DIP switch](#) setting. The standard specifications allow operation in three modes: “USB mode”, “DisplayPort mode”, and “Updater mode”.



In USB mode, video files (uncompressed .avi or .frm files) stored on the PC can be transferred to the board via USB 3.2 Gen2/Gen1 using our board software (NVFilePlayer). Any video signal can be input from the PC to devices or ICs with MIPI CSI-2 input. The timing, pixel format, FSYNC synchronous output, and other settings for the video signal output from the board are configured using software on the PC.

In DisplayPort mode, the video input via DisplayPort is converted to the resolution, timing, and pixel format saved in the board’s SPI-ROM, and output as a MIPI CSI-2 signal.

In Updater mode, the firmware and FPGA can be updated via USB. Be sure to start the board in updater mode before performing the update.

1.1. SVL-03-GEN Functions

USB mode: Video files on a computer -> MIPI CSI-2 video signal conversion

DisplayPort mode: DisplayPort input -> MIPI CSI-2 video signal conversion

Updater mode: Update the board firmware / FPGA

1.2. Specifications (USB Mode)

Power: USB bus supply (External power supply also available) / +5V 0.83A typ.

Input Standards: USB Vendor Class, Gen2 max. 2.4 Gbps

Input Resolution: Same as the output resolution

Input Pixel Format (USB side): YUV4:2:2 (8bit), RGB24

Output Standards: MIPI CSI-2 video signals (Data 1 - 4 lanes + 1 clock lane)
max. 1500 Mbps/Lane

Output Resolution: max. 8190x4095 pixel

Output Pixel Format: YUV4:2:2 (8bit), Raw8, Raw10, Raw12, Raw16, Raw20, RGB24

Output Frame Rate: Any value

1.3. Specifications (DisplayPort Mode)

Power: USB bus supply (External power supply also available) / +5V 0.9A typ.

Input Standards: DisplayPort 1.1a, max. 2.7 Gbps/Lane x2L

Input Resolution: max. 8190x4095 pixel

Input Pixel Format: RGB24

Output Standards: MIPI CSI-2 video signals (Data 1 - 4 lanes + 1 clock lane)
max. 1500 Mbps/Lane

Output Resolution: max. 8190x4095 pixel

Output Pixel Format: YUV4:2:2 (8bit), RGB24, (Raw8,10,12,16,20) *1

*1. Output in RAW format is not supported as standard.

1.4. Board Specification

Item	Content	Remark
Video Input Interface	USB3.2 Gen2 (Windows) DisplayPort 1.1a	
Video Output Interface	MIPI CSI-2 video signal	Non-Continuous /Continuous Clock supported 4 data lanes + 1 clock lane
Input Resolution	Max. 8190 x 4095 pixel (USB mode) Within 2.4 Gbps (DisplayPort mode) Within 5.4 Gbps	(DisplayPort mode) – YUV4:2:2 (8bit): max. 2560x1440@60fps – RGB24: max. 1920x1080@90fps – Customization is required for 4K-30fps input. – Dual-Mode (DP++): Not supported – DPCP: None
Output Resolution	Max. 8190 x 4095 pixel	(DisplayPort mode) It is also possible to cut out any area and output it.
Sync Signal	FS / FE	LS / LE are optional.
MIPI Data Lane	1, 2, 4 lanes	3 lane output is not supported.
Data Rate Per Lane	600 ~ 1500 Mbps	Standard: Data rates lower than 600 Mbps are not supported.

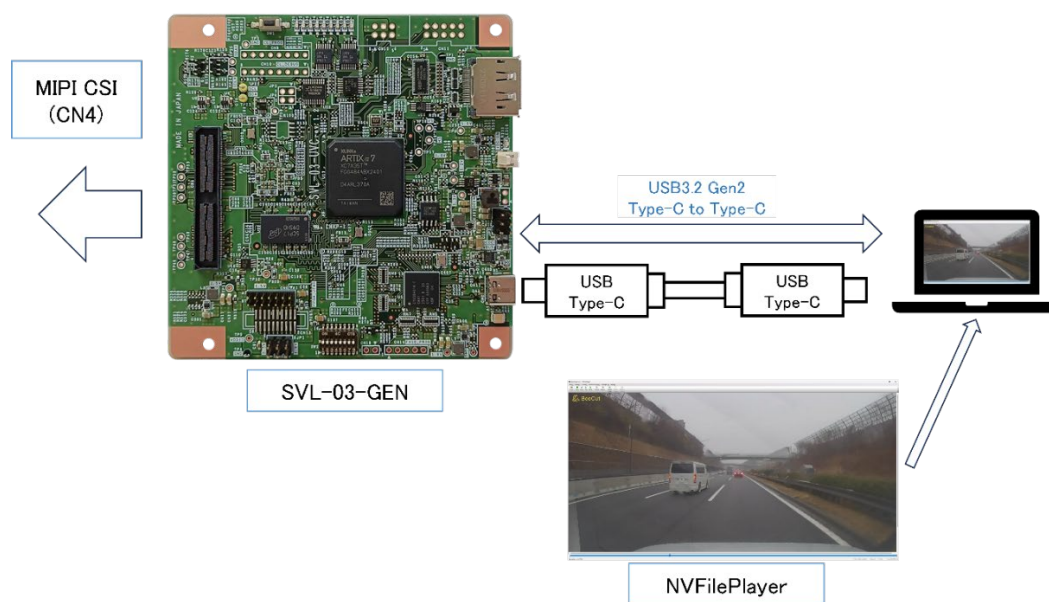
Clock Rate		300 ~ 750 MHz	
Supported Pixel Formats		YUV4:2:2 (8bit) / RGB24 / Raw8 / Raw10 / Raw12 / Raw16 / Raw20	
Other IF	I2C	1 system Frequency: 100 / 200 / 400 kHz / 1MHz (1MHz is HW only)	Voltage level follows VDDIO.
	GPIO	16bit, IN/OUT direction control for each bit. Direct connection to FPGA.	Voltage level follows VDDIO.
	Synchronous Connector	Synchronous signal input and output. Direction control of IN / OUT.	Fixed at 1.8V.
Power	Input Power	USB bus power / Dedicated 2pin connector	The dedicated 2pin connector has two input range selections: 5V to 5.5V / 6.5V to 16V by a jumper pin. USB bus power can be disconnected with a jumper pin. CN1: Sub Power Connector
	Output Power	VDDIO output (1.8V, 2.5V, 3.3V) 1.2V, 3.3V, 5V output	VDDIO:IO power supply setting Shared with internal power supply. Current rating 1.2A (VDDIO), 1.2A (3.3V), 3.0A (1.2V, 5V)
	Protection Elements	eFuse 6V / 4.8A (TCKE805NL)	Recovery by turning board power OFF when shut down.
Other Functions		Video output timing setting: pixel clock unit (including blank).	<ul style="list-style-type: none"> •Automatically transmit I2C setting at startup from ROM. •Virtual Channel 0~3. •Image clipping.
Interface Connector		120pin (QSH-060-01-L-D-A)	
FPGA		Artix-7 (XC7A35T) CrossLink (LIF-MD6000)	
Frame Memory		256MB (DDR3 SDRAM)	
USB	Device Controller	Infineon EZ-USB™ FX10	
	Connector	USB3.2 Gen2 Type-C	

Board Dimensions	101.6 x 101.6 x 24.0 [mm]	Length x Width x Height (Height includes spacer (10mm))
Attached Software (Windows)	NVFilePlayer, SVMCtl, SVMUpdater	
Examples of Supported Serializer Boards	GMO-9295A-F GMO-96717 and so on.	

2. USB Mode Operation Details

This chapter describes USB mode (USB input, MIPI CSI-2 output).

2.1. Connection Example in USB Mode



2.2. Setup Instructions in USB Mode

- Input Settings

Input settings are configured using the PC software “NVFilePlayer”. Uncompressed video data, such as AVI files, can be imported and sent to the SVL-03-GEN. For instructions on using NVFilePlayer, please refer to the “NVFilePlayer Software Manual”.

- Output Settings

Output settings are configured using the PC software “NVFilePlayer”. It is possible to configure settings related to various video signals, such as video timing and pixel format. For instructions on using NVFilePlayer, please refer to the “NVFilePlayer Software Manual”.

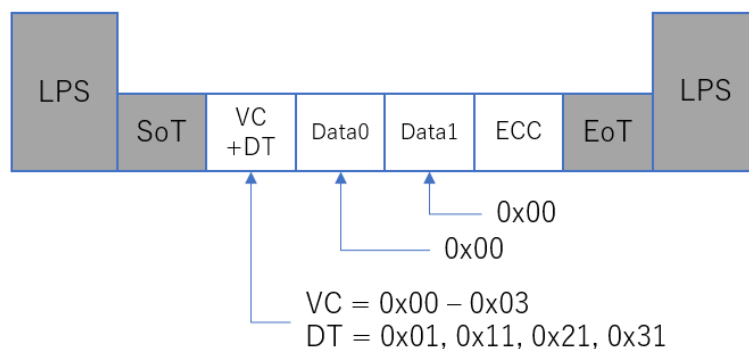
2.3. USB Input Data Rate

There are two types of transfer operations in USB mode. The first is to store frame data in the on-board frame memory in advance and loop output only the number of stored frames. The other is to transfer frames on demand from the PC. When transferring frames on demand from the PC, the output data rate is limited to the input slew rate listed [Specifications \(USB Mode\)](#). For information on setting these operations, refer to the “NVFilePlayer_Software Manual”.

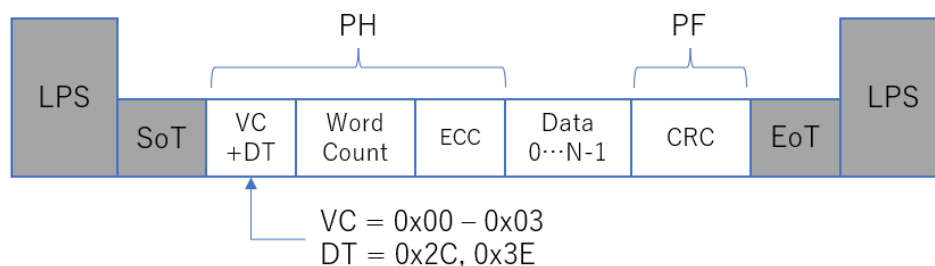
2.4. Output Format

Details of the MIPI CSI-2 signals output by this board are described below.

Short Packet



Long Packet

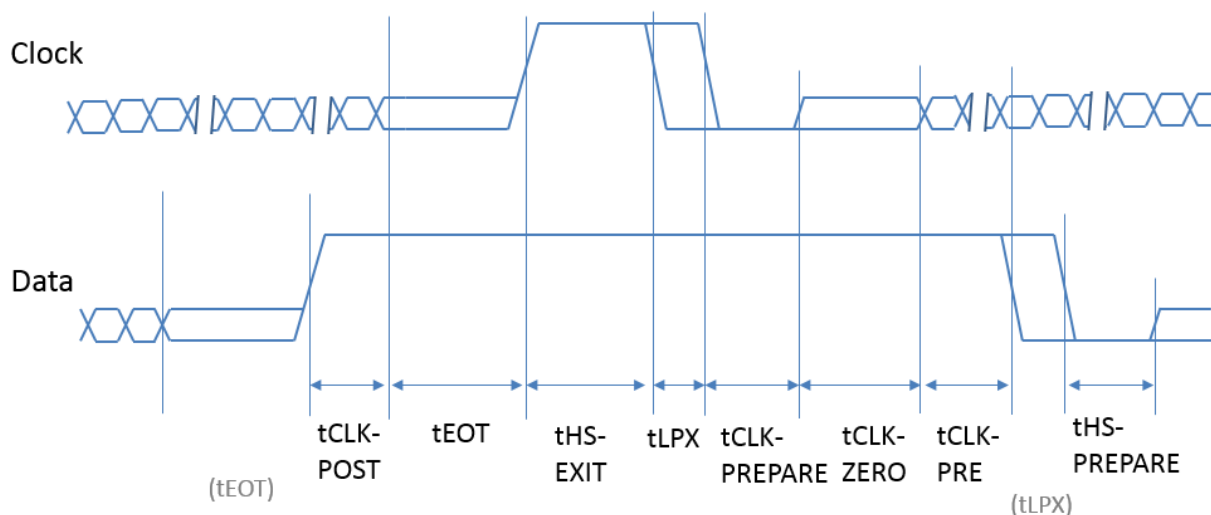


The pixel formats and long packet data types supported by this board are shown in the table below. The Input AVI Format column shows the pixel format of the input AVI file when operating this board with NVFilePlayer.

Pixel Format	Data Type (DT)	Input AVI Format (NVFilePlayer)
YUV4:2:2 8bit	0x1E	UYVY, YUY2
RGB24 (RGB888)	0x24	DIB (upside down)
Raw8	0x2A	UYVY
Raw10	0x2B	UYVY
Raw12	0x2C	UYVY
Raw16	0x2E	UYVY
Raw20	0x2F	DIB (flip vertically)

- Even if DIB or RGB AVI data is read, the data is always sent from the beginning of the AVI file first.

2.5. MIPI Output Timing

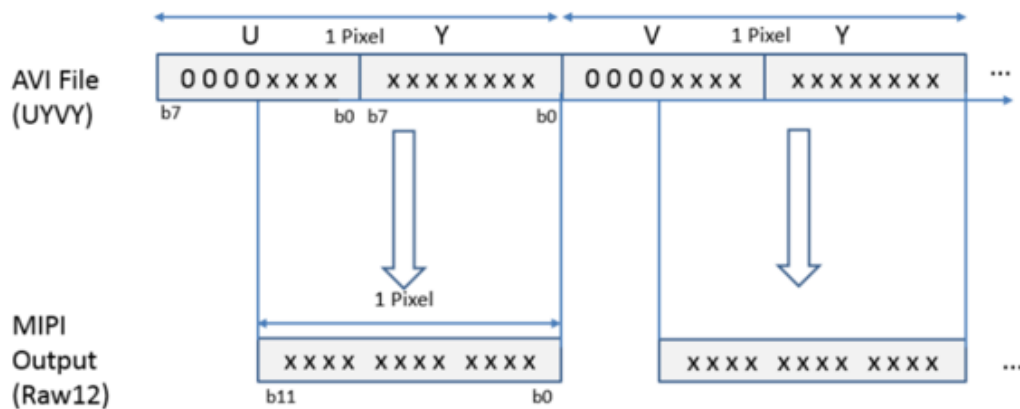


Timing	Measured Value - 1	Measured Value - 2	Measured Value - 3
$t_{\text{CLK-POST}}$	720ns	360ns	220ns
t_{EOT}	210ns	105ns	75ns
$t_{\text{HS-EXIT}}$	-	-	-
t_{LPX}	95ns	95ns	95ns
$t_{\text{CLK-PREPARE}}$	75ns	75ns	50ns
$t_{\text{CLK-PREPARE}} + t_{\text{CLK-ZERO}}$	1050ns	525ns	310ns
$t_{\text{CLK-PRE}}$	300ns	150ns	110ns
$t_{\text{HS-PREPARE}}$	55ns	55ns	55ns

- Measured Value - 1: Indicates the actual measured value at 500Mbps/lane output.
- Measured Value - 2: Indicates the actual measured value at 1000Mbps/lane output.
- Measured Value - 3: Indicates the actual measured value at 1500Mbps/lane output.
- Fine-tuning of each timing is possible as a custom request.

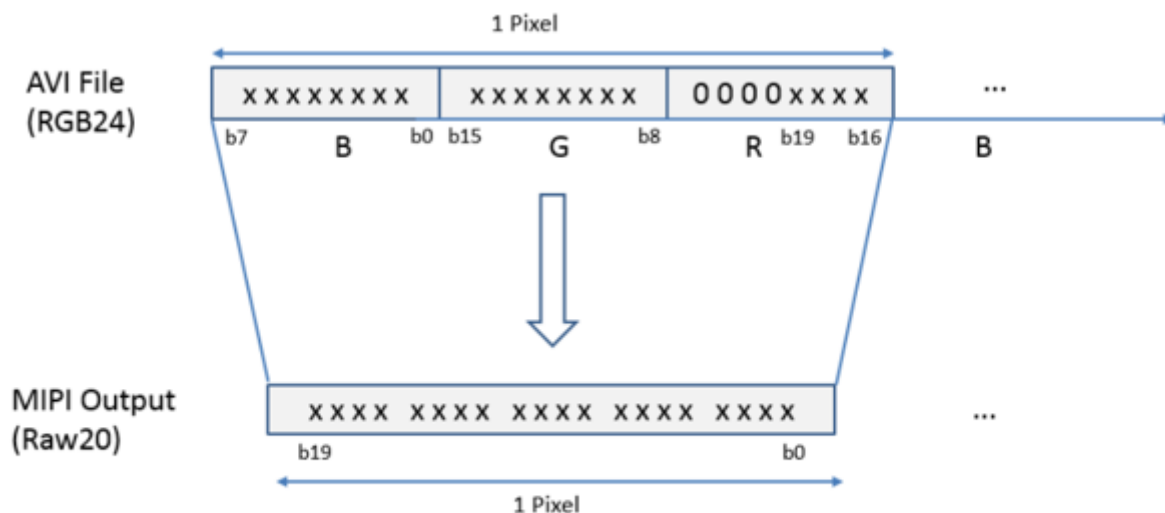
2.6. Processing on RAW Video File Input

This board supports Raw8, Raw10, Raw12, Raw16, and Raw20 as Raw output formats. Since the Windows OS standard does not support the Raw format, if Raw format output is selected when operating in USB mode, the input file will conform to the format saved by our capture board. In other words, the MIPI signal will be output assuming that valid data is stored as part of the YUV or RGB format input data. Please see below for details on the data format.



The host side treats it as UYVY data and pads the upper bits with 0.
(The bit rate is 4/3.)

(The above diagram is for Raw12, but the same applies to other Raw formats.)



The host side treats it as RGB24 data and pads the upper bits with 0.
(The bit rate is 6/5.)

For RGB24 and Raw20 output, the input AVI file supports RGB24 format. The pixel order output by this board will always be the same as the byte array in the AVI file. When using an RGB24 AVI file to emulate a standard camera, the vertical orientation of each frame in the AVI file must be stored from the top left to the bottom right, unlike VFW's RGB24 (bottom left to top right). In other words, if an upside-down RGB24 format AVI file is input, the output signal from the board will be output in the order of the top left pixel to the bottom right pixel.

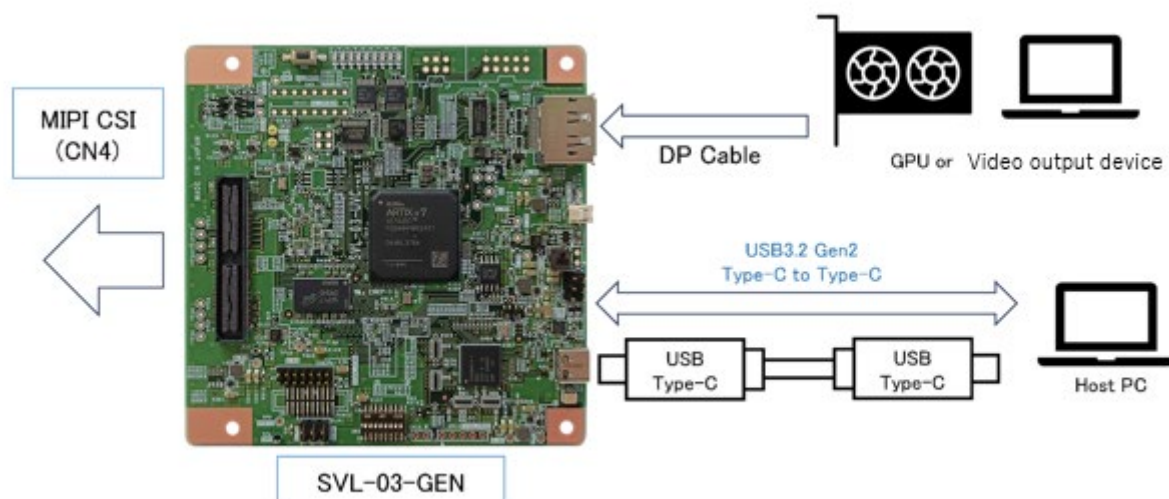
2.7. Power Consumption in USB Mode

When inputting and outputting 1920x1080/60FPS YUV422-8bit video without connecting a target, the current consumption is approximately 830mA for a 5V power input. If a target is connected and a video is imported, the current consumption will increase even further. Therefore, please use an AC adapter or USB cable with sufficient current capacity for power supply.

3. DisplayPort Mode Operation Details

This chapter describes DisplayPort mode (DisplayPort input, MIPI output).

3.1. Connection Example in DisplayPort Mode



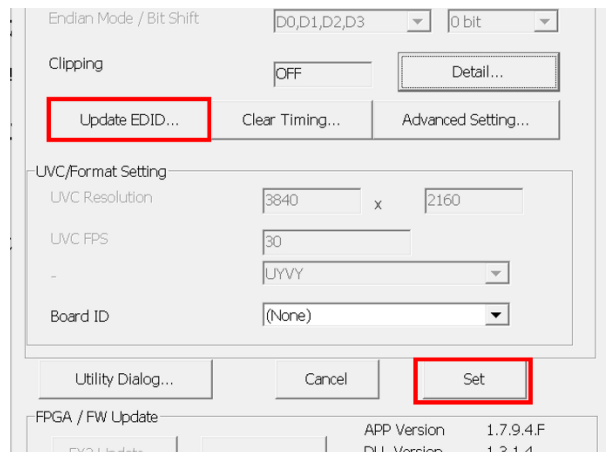
3.2. Input Setting in DisplayPort Mode

- Writing an EDID File

Use the PC software “SVMCtl” to write the EDID. Because the SVL-03-GEN operates as a DisplayPort Sink (receiver), EDID (Extended Display Identification Data) must be written to the board to notify the DisplayPort Source (transmitter) of the receiver’s supported resolutions and timing.

The EDID file must be a 256byte binary file that includes Extended-EDID, or a 128byte binary file that does not. Generate it using a general-purpose EDID editor.

If an EDID file has already been written to the board, click the “Clear EDID...” button to clear the file, then click the “Update EDID...” button to select the data to write. After writing is complete, click the “Set” button to write the data to the SPI-ROM on the board. The written EDID will be applied when the board is restarted. For details, refer to the SVMCtl software manual. If an EDID file has not been written to the board, the 1920x1080/60FPS RGB888 input setting will be applied.

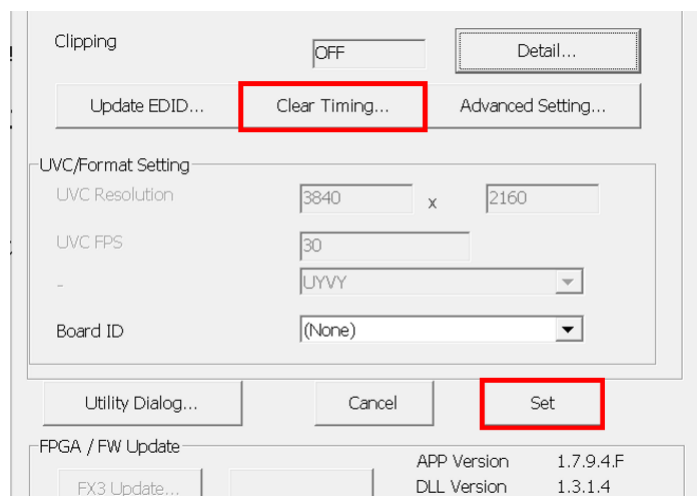


3.3. Output Setting in DisplayPort Mode

- Writing a Video Output Timing File

Use the PC software “SVMCtl” to write the output timing file. To output signals with custom video timing in DisplayPort mode, write output timing data. Output timing data (.svo file) can be created using “TimingGenSVO06.exe” included in the app folder.

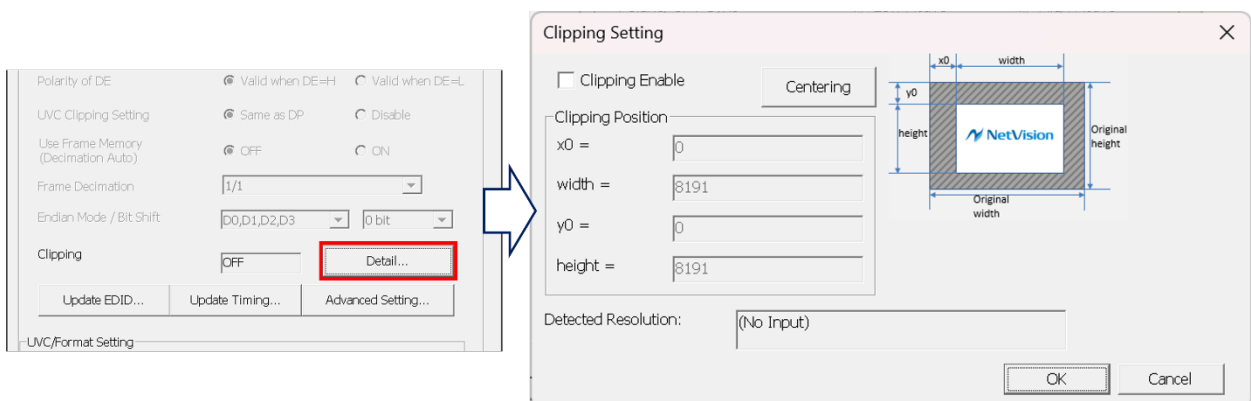
If the output timing data has already been written to the board, the “Clear Timing...” button will be displayed. Click this button to clear the data. If the output timing data has not been written, the “Update Timing...” button will be displayed. Click this button and select the .svo file created using “TimingGenSVO06.exe”. If a timing settings file has not been written, the output settings of 1920x1080/60FPS YUV422-8bit will be applied.



- Clipping Function

This board is equipped with a clipping function that can be used to output at a resolution lower than the input resolution specified in the EDID. By setting any area in Clipping Position and adjusting the timing accordingly, the clipped video will be output.

Please set the same value for the clipping settings and the resolution settings in the output timing data.



3.4. Color Conversion Formula

The RGB and YUV conversion formula is bt.601. Input/Output scaling (Limited/Full conversion) can be set using SVMCtl.

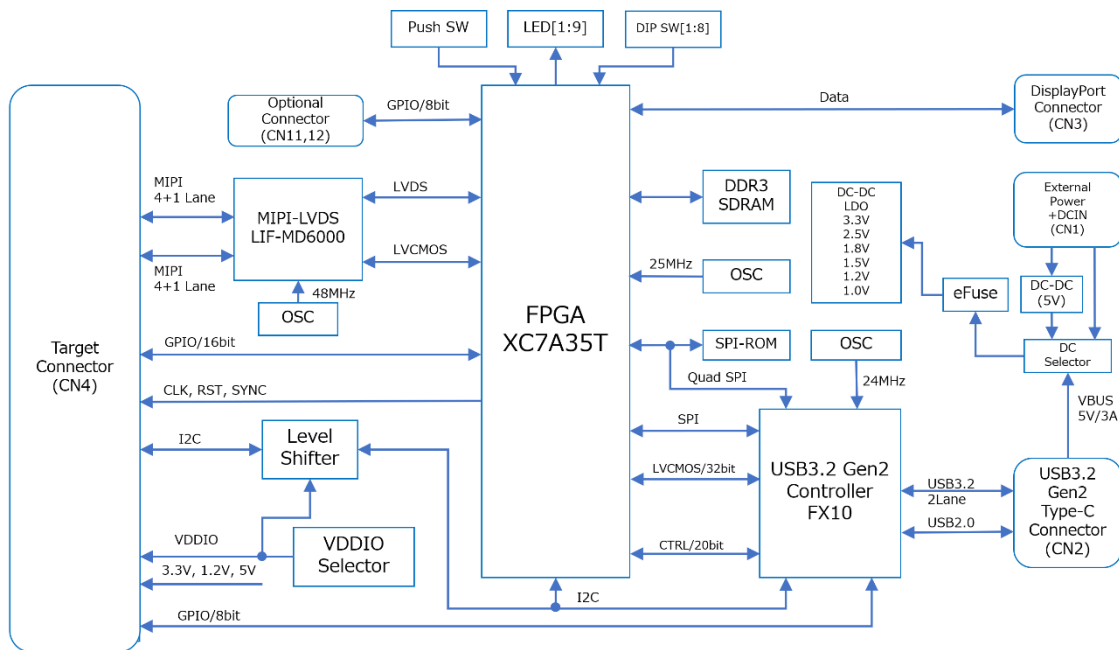
3.5. Power Consumption in DisplayPort Mode

When operating at 1920x1080/60FPS, RGB888 input, YUV422-8bit output without connecting a target, the current consumed is approximately 900mA for a 5V power input. When connecting a target and capturing video, the current consumption will increase even more, so please supply power using an AC adapter or USB cable with sufficient current capacity.

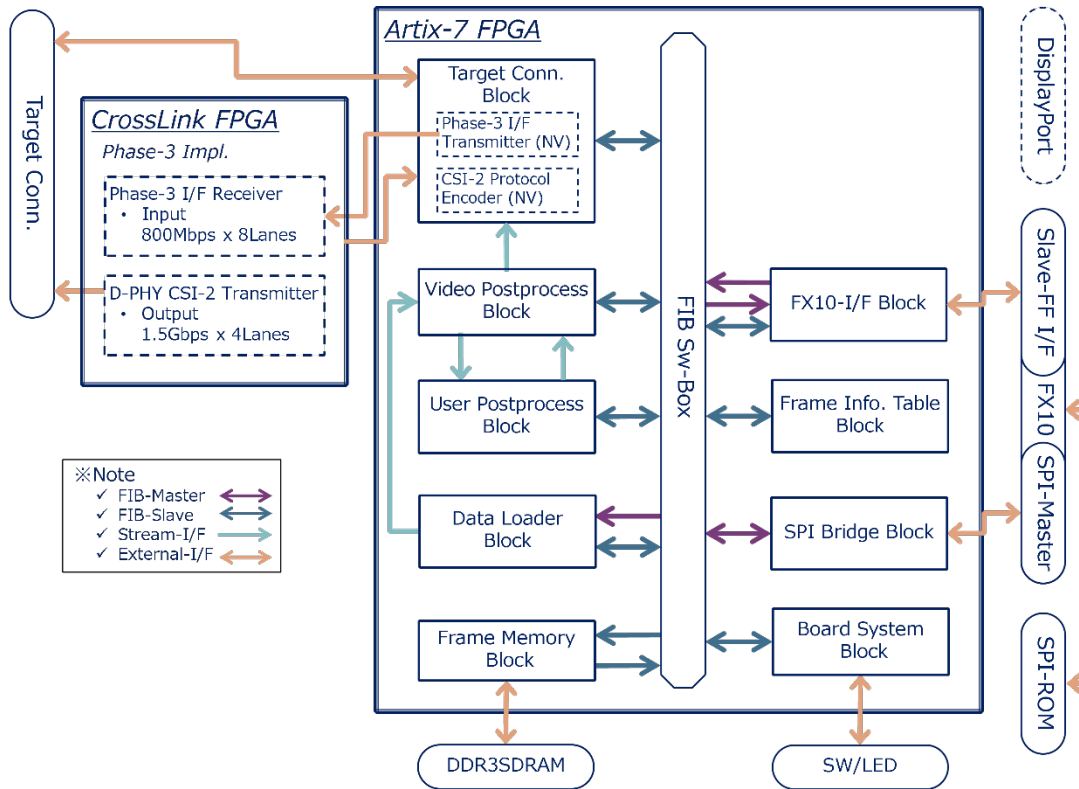
4. Block Diagram of SVL-03

The block diagrams of the SVL-03 are shown below.

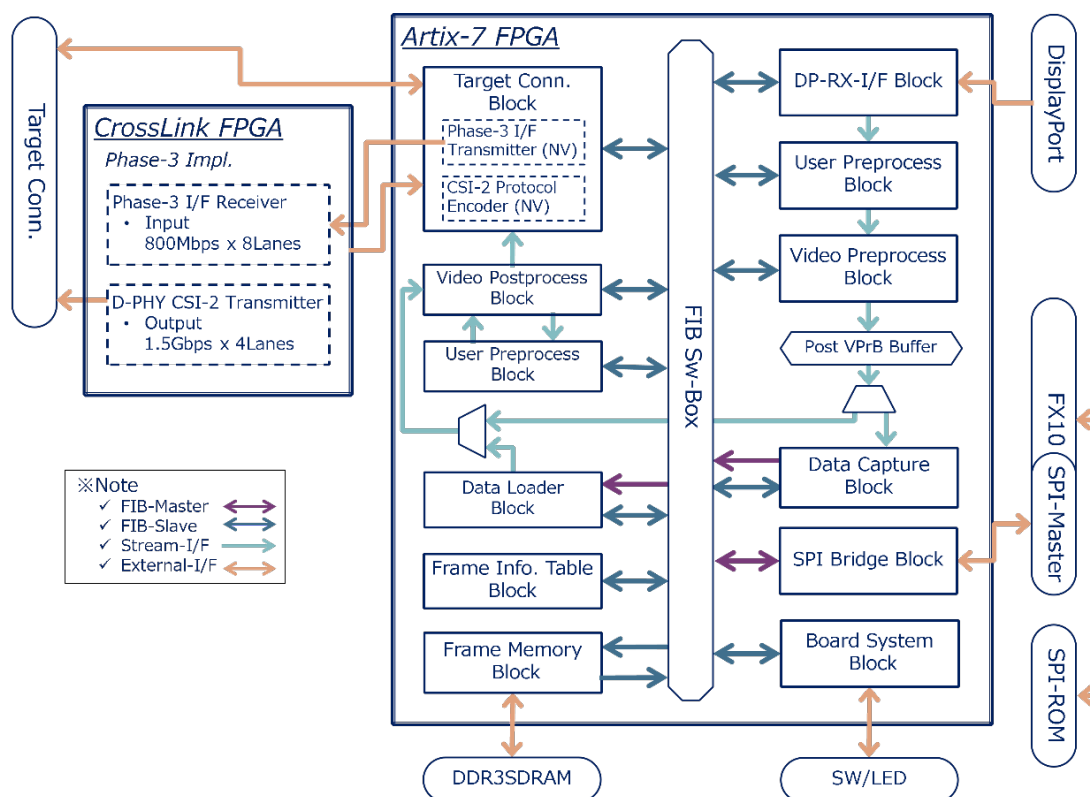
4.1. Block Diagram



4.2. FPGA Internal Block Diagram in USB Mode



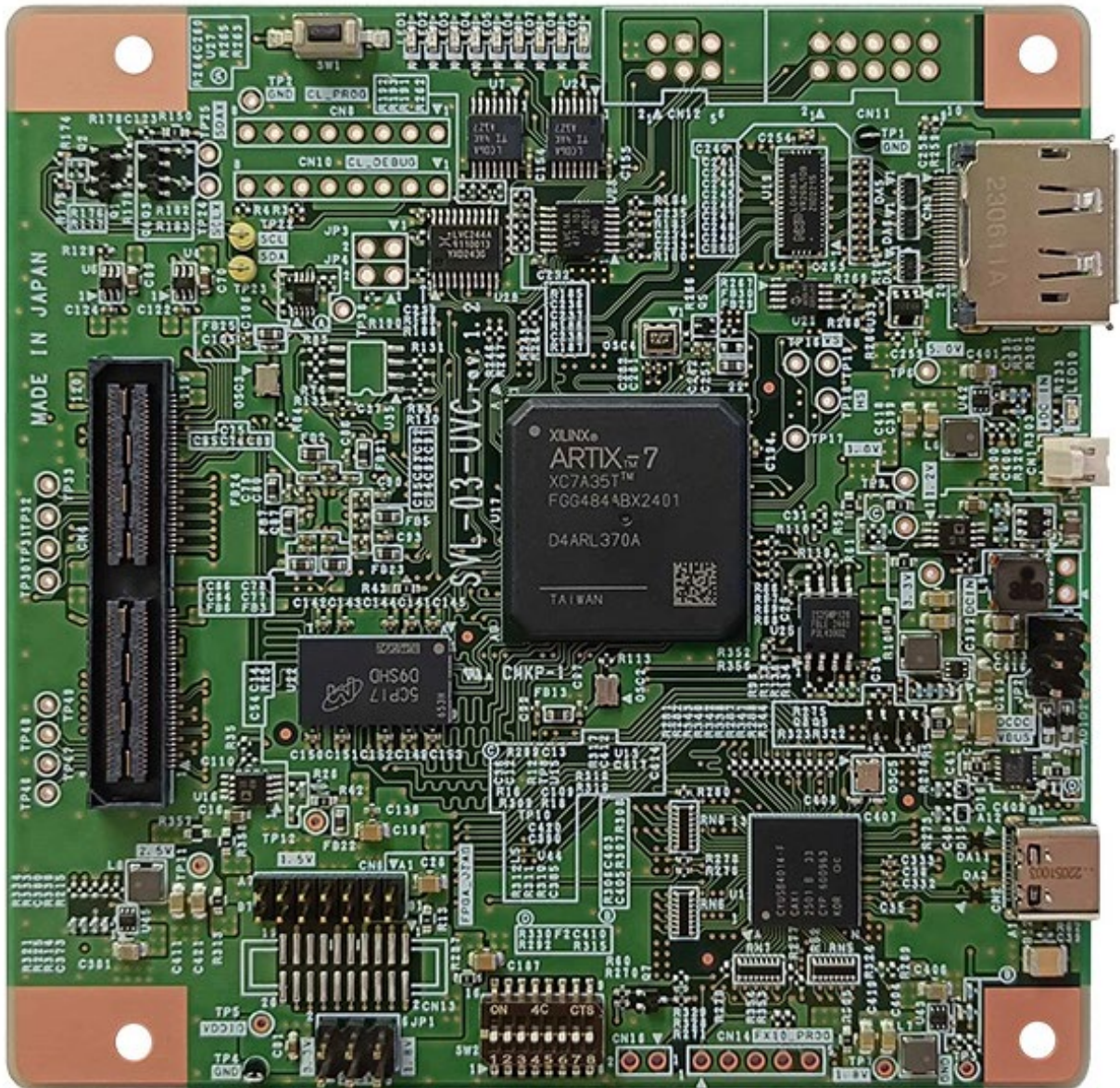
4.3. FPGA Internal Block Diagram in DisplayPort Mode



5. Board External and Dimensions

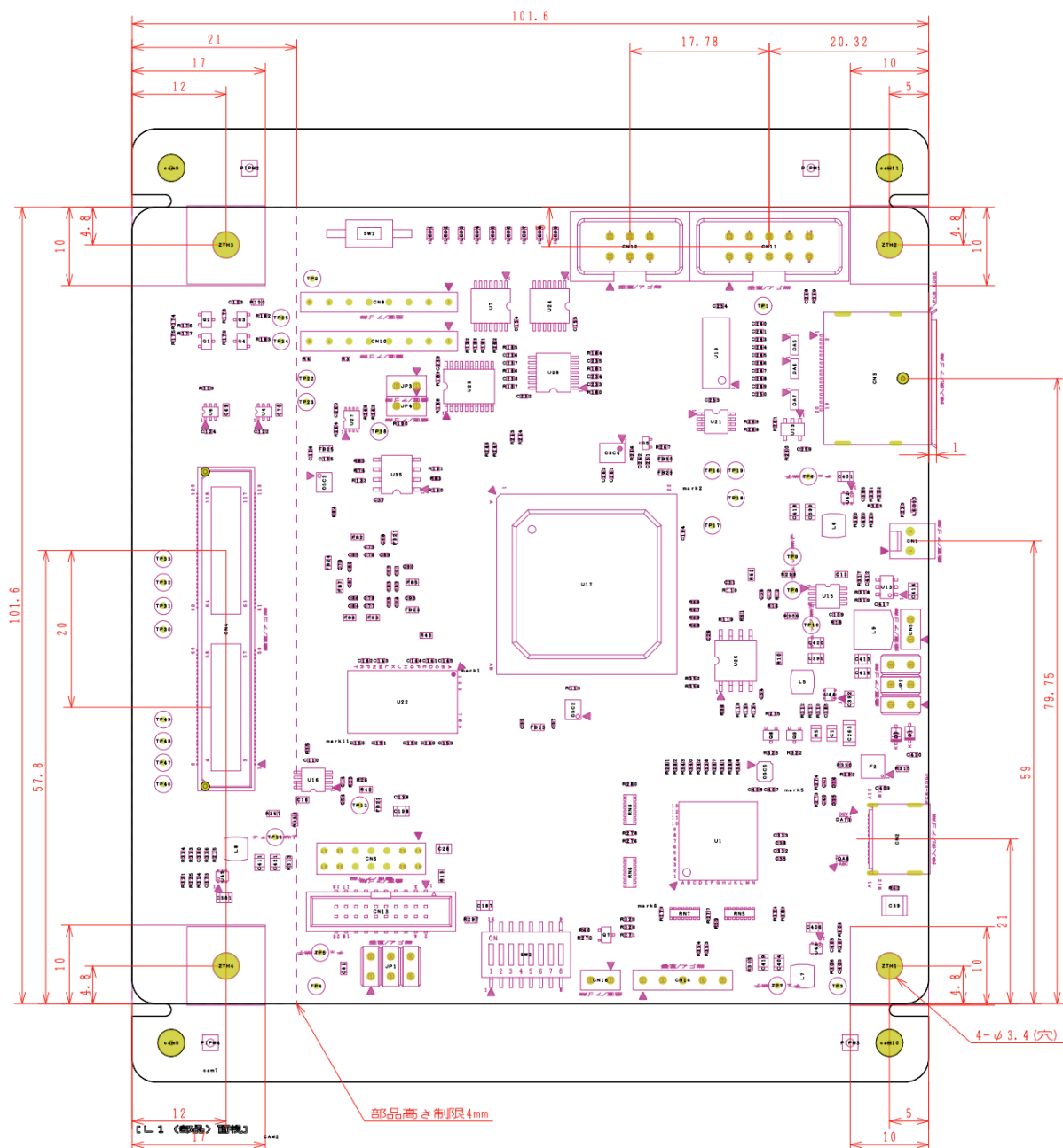
The photo and the outline diagram of the SVL-03 are shown below.

5.1. Board Photo (rev.1.2)



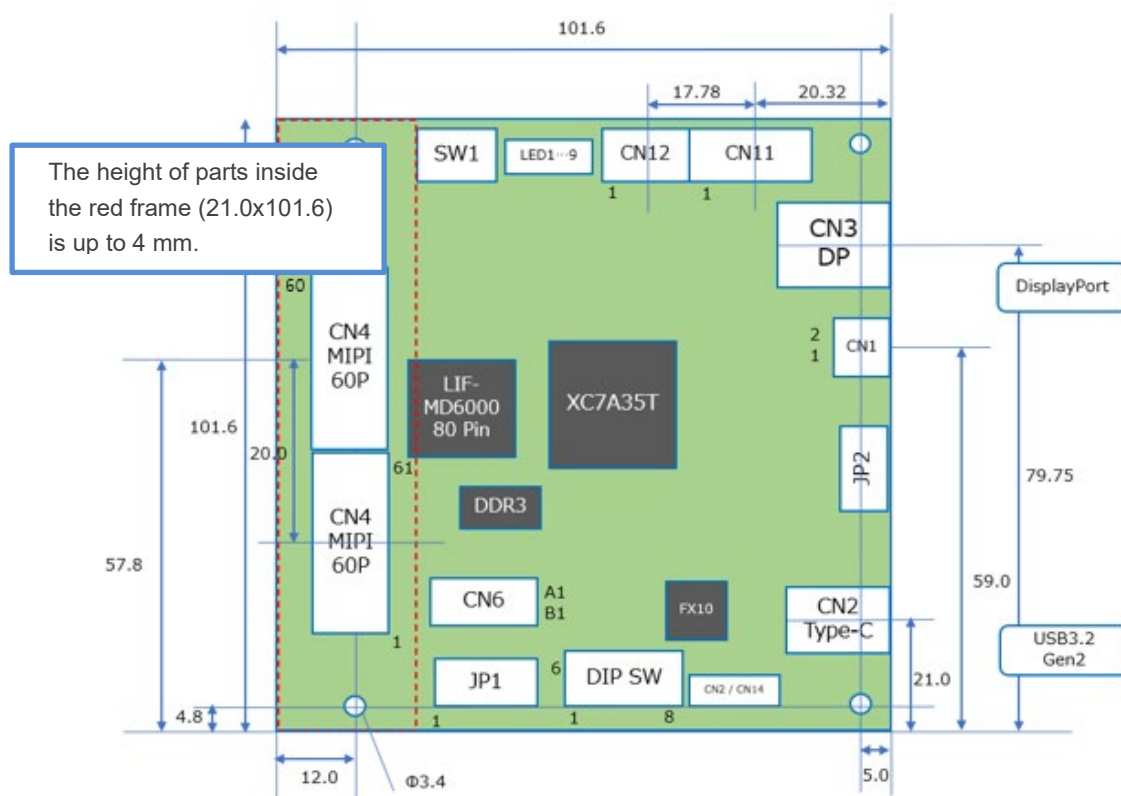
5.2. Drawing

The dimensional drawing of the SVL-03 is shown below. On the actual board, the 10 mm sections extending to the VCUT at the top and bottom are not included. The external dimensions are 101.6mm□, which is standard for all SV series boards.



The schematic diagram shows two main components: SerDes and SVL-03. SerDes is represented by a green rectangle with two teal-colored connectors on its left side. SVL-03 is represented by a larger green rectangle to the right of SerDes. A black rectangle is located at the top left of the SerDes area, and a light gray rectangle is at the top right. Two labels, CN2 and CN3, are positioned to the right of the SVL-03 component. Below the schematic, a physical layout is shown with a dimension line indicating a distance of $< 21\text{mm}$ between two points.

The SVL-03 is used by connecting a target connection board to connector CN4 as shown above. This connection board partially overlaps with the SVL-03, **but the overlapping area must not exceed 21 mm from the edge of the SVL-03**. This area is outlined in the red dotted box below. If using a connection board that extends beyond this frame, ensure that its shape is compatible and use a tall connector to allow proper connection of both boards.



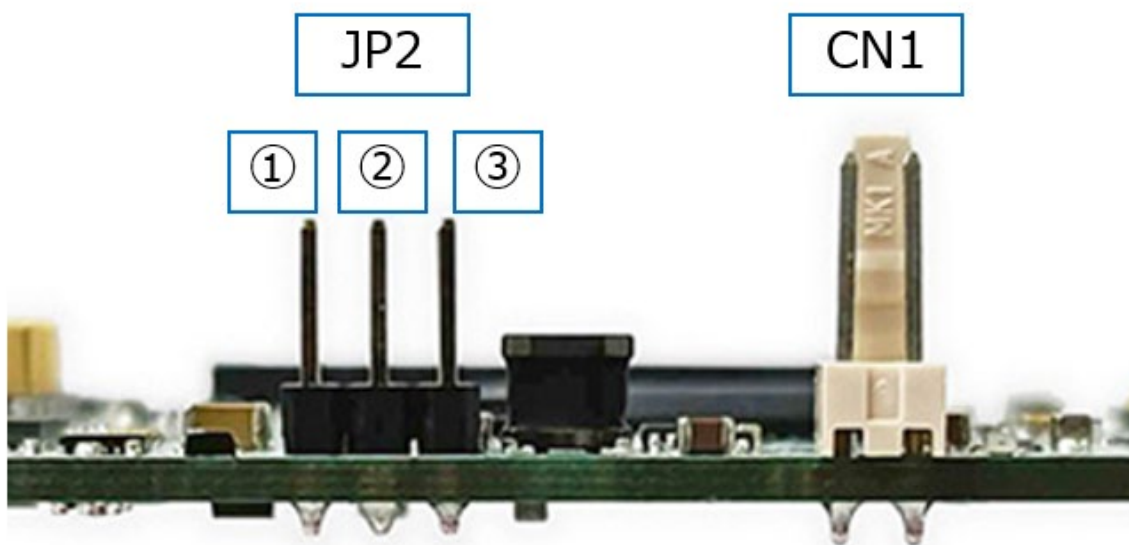
6. Connector Specifications

This chapter describes the specifications of the main connectors used for normal operation when connecting to the target. Other connectors are described in the [Appendix](#).

6.1. CN1: Sub Power Connector

This power connector is used when the USB bus power is insufficient to meet the power supply requirements, or when USB bus power is not used. CN1 supports input ranges of DC5.0-5.5V and DC6.5V-16V, with the input range selected via JP2 (② and ③ in the figure below). It is also possible to disconnect the USB bus power (① in the figure below).

For DC5.0-5.5V input settings, the external power supply voltage is directly supplied to the board. For DC6.5V-16V input settings, the step-down circuit converts the external power supply voltage to 5V, and then it is supplied to the board. The power input is connected to the bus power (VUSB) from the USB connector via a diode OR circuit and is used as the board's internal power supply.

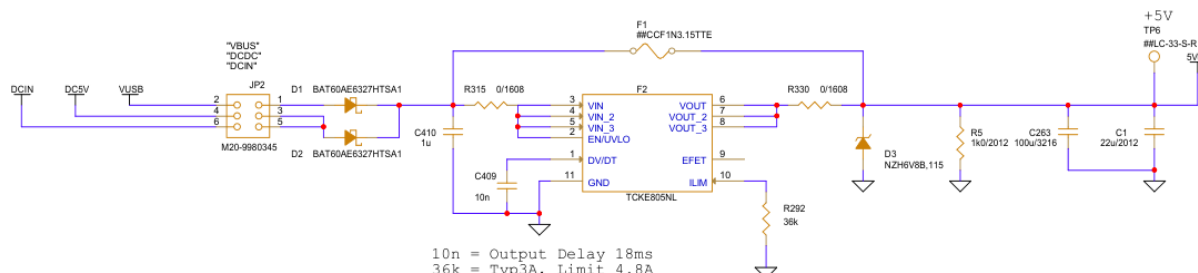


- Jumper Settings

JP2 Pin No	Open	Short-Circuit
USB Bus Power Selection ①	USB bus power is not used.	USB bus power is used as the board power supply.
DC6.5-16V Range Selection ②	DC6.5V - 16V is not used.	A voltage of 5V converted from an external power supply by the step-down circuit is used as the board power supply.
DC5.0-5.5V Range Selection ③	DC5.0V - 5.5V is not used.	The external power supply (5.0V-5.5V) is directly used as the board power supply.

- Do not supply external power when both jumpers ② and ③ are shorted.
- Do not supply more than DC5.5V from the external power when jumper ③ is shorted.
- At the time of shipment, jumpers ① and ③ are shorted.

- Input Power Supply Schematic.



6.2. CN2: USB Type-C Connector

This connector is a USB Type-C receptacle that connects to the host PC. Please note the following:

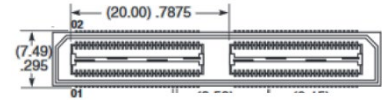
- Use a host PC compatible with USB 3.2 Gen2/Gen1 Type-C and a Type-C to Type-C cable. This board does not support USB 2.0, so it will not work with a Type-C cable, which only supports USB 2.0. Please note that if connected via USB 2.0, this board will be recognized as an unknown USB device.
- Type-A (host PC) to Type-C (SVL-03) cables are not officially supported by the USB I/F standard. Using such a cable may damage the host PC circuit due to overcurrent or result in insufficient power supply to the board, causing system instability.
- By using a Type-A to Type-C cable, it is possible to operate the device using by opening the USB bus power with JP2 setting and supply power from CN1. However, operation is not guaranteed in this case. For details on CN1 and JP2, refer to [CN1: Sub Power Connector](#).

• USB Type-C Connector Pin Assignment

Connector		1054500101					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
A1	GND	-	Ground	A2	TX1+	OUT	USB3.2 differential pair +
A3	TX1-	OUT	USB3.2 differential pair -	A4	VBUS	+	Bus power
A5	CC1	-	5.1k Ω pulldown	A6	D+	I/O	USB2.0 differential pair +
A7	D-	I/O	USB2.0 differential pair -	A8	SBU1	-	Disconnected
A9	VBUS	+	Bus power	A10	RX2-	IN	USB3.2 differential pair -
A11	RX2+	IN	USB3.2 differential pair +	A12	GND	-	Ground
B1	GND	-	Ground	B2	TX2+	OUT	USB3.2 differential pair +
B3	TX2-	OUT	USB3.2 differential pair -	B4	VBUS	+	Bus power
B5	CC2	-	5.1k Ω pulldown	B6	D+	I/O	USB2.0 differential pair +
B7	D-	I/O	USB2.0 differential pair -	B8	SBU2	-	Disconnected
B9	VBUS	+	Bus power	B10	RX1-	IN	USB3.2 differential pair -
B11	RX1+	IN	USB3.2 differential pair +	B12	GND	-	Ground

6.3. CN4: Target Connector

This connector is used to connect to the target device.



Main Port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
61	D1_N	OUT	MIPI lane1 output -	62	GPIO0	IO	GPIO 0
63	D1_P	OUT	MIPI lane1 output +	64	GPIO1	IO	GPIO 1
65	GND	-		66	GND	-	
67	D3_N	OUT	MIPI lane3 output -	68	GPIO2	IO	GPIO 2
69	D3_P	OUT	MIPI lane3 output +	70	GPIO3	IO	GPIO 3
71	GND	-		72	GND	-	
73	CLK_N	OUT	MIPI clock output -	74	GPIO4	IO	Connect to TP30 and use as Trigger signal input/FSYNC signal input
75	CLK_P	OUT	MIPI clock output +	76	GPIO5	IO	GPIO 5 (Connected to TP31)
77	GND	-		78	GND	-	
79	D2_N	OUT	MIPI lane2 output -	80	GPIO6	IO	GPIO 6 (Connected to TP32)
81	D2_P	OUT	MIPI lane2 output +	82	GPIO7	IO	GPIO 7 (Connected to TP33)
83	GND	-		84	GND	-	
85	D4_N	OUT	MIPI lane4 output -	86	GPIO8	IO	GPIO 8
87	D4_P	OUT	MIPI lane4 output +	88	GPIO9	IO	GPIO 9
89	GND	-		90	GND	-	
91	SCL	IO	I2C SCL signal line	92	GPIO10	IO	GPIO 10
93	SDA	IO	I2C SDA signal line	94	GPIO11	IO	GPIO 11
95	GND	-		96	GND	-	
97	GND	-		98	NC	-	
99	GND	-		100	NC	-	
101	GND	-		102	GND	-	

103	VSYNC	IO	VSYNC input/output (Reserved)	104	GPIO12	IO	Available as VSYNC output (USB mode only)
105	HSYNC	IO	HSYNC input/output (Reserved)	106	GPIO13	IO	Available as H SYNC output (USB mode only)
107	GND	-		108	GND	-	
109	CK	OUT	Clock output (Reserved)	110	GPIO14	IO	GPIO 14
111	RST	OUT	Reset output (L : Reset)	112	GPIO15	IO	GPIO 15
113	GND	-		114	GND	-	
115	VDDIO	POW	IO power output	116	1V2	POW	1.2V power output
117	3V3	POW	3.3V power output	118	3V3	POW	3.3V power output
119	GND	-		120	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

- Lane numbers are denoted as 1-4 instead of 0-3.

Extension Port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	D1_N	OUT	MIPI lane5 output -	2	NC	-	(Connected to TP46)
3	D1_P	OUT	MIPI lane5 output +	4	NC	-	(Connected to TP47)
5	GND	-		6	GND	-	
7	D3_N	OUT	MIPI lane7 output -	8	NC	-	(Connected to TP48)
9	D3_P	OUT	MIPI lane7 output +	10	NC	-	(Connected to TP49)
11	GND	-		12	GND	-	
13	CLK_N	OUT	MIPI clock2 output -	14	MCU_GP IO0	IO	(Reserved)
15	CLK_P	OUT	MIPI clock2 output +	16	MCU_GP IO1	IO	(Reserved)
17	GND	-		18	GND	-	
19	D2_N	OUT	MIPI lane6 output -	20	MCU_GP IO2	IO	(Reserved)

21	D2_P	OUT	MIPI lane6 output +	22	MCU_GP IO3	IO	(Reserved)
23	GND	-		24	GND	-	
25	D4_N	OUT	MIPI lane8 output -	26	MCU_GP IO4	IO	(Reserved)
27	D4_P	OUT	MIPI lane8 output +	28	MCU_GP IO5	IO	(Reserved)
29	GND	-		30	GND	-	
31	SCL	IO	I2C SCL signal line	32	MCU_GP IO6	IO	(Reserved)
33	SDA	IO	I2C SDA signal line	34	MCU_GP IO7	IO	(Reserved)
35	GND	-		36	GND	-	
37	NC	-		38	NC	-	
39	NC	-		40	NC	-	
41	GND	-		42	GND	-	
43	5V0	POW	5V power output	44	NC	-	
45	5V0	POW	5V power output	46	NC	-	
47	GND	-		48	GND	-	
49	NC	-		50	NC	-	
51	NC	-		52	NC	-	
53	GND	-		54	GND	-	
55	VDDIO	POW	IO power output	56	5V0	POW	5.0V power output
57	3V3	POW	3.3V power output	58	3V3	POW	3.3V power output
59	GND	-		60	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

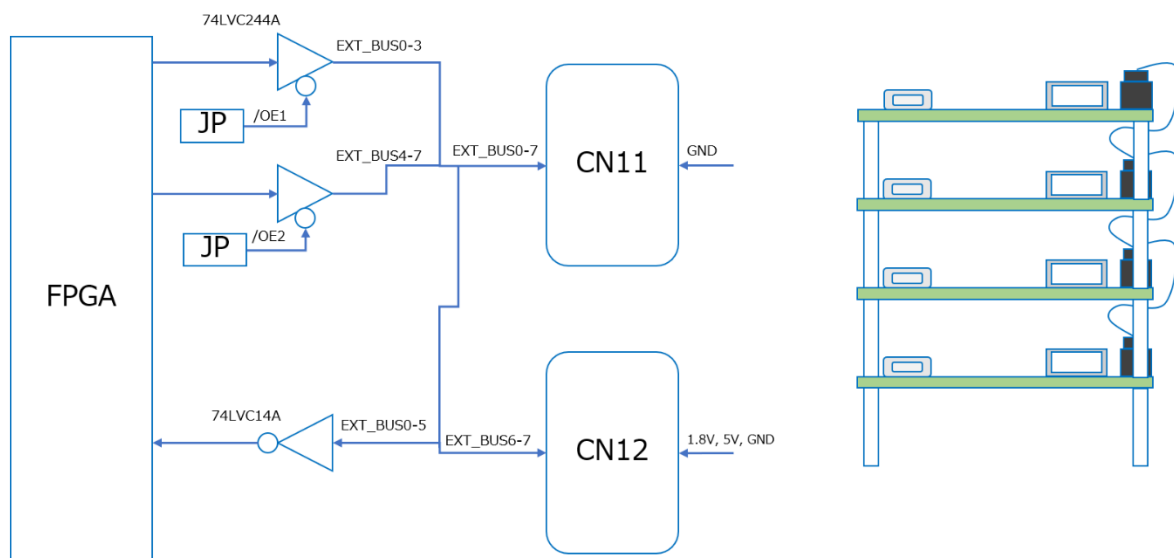
- The connector position and pin assignment are compatible with our previous boards, such as the SVO-03-MIPI. Therefore, interface boards designed for our previous boards can be connected.
- MIPI lanes 5-8 are not supported in the standard version.
- If the expansion port side (1-60P) is not used, it can be treated as a 60pin connector (Connection target: QTH-030-01-L-D-A). In this case, only the main port side (61-120P) should be used.
- The HSYNC and VSYNC pins are reserved for customization and have no function in the standard version.

- The default state of GPIO pins is Hi-Z (FPGA internal pull-up). The direction and level of each pin are set by FPGA registers. The FPGA internal pull-up cannot be changed by setting.
- The IO voltages for each single-ended port of the FPGA are determined by jumper JP1.
- The MCU_GPIO pin is a reserved function. The default state of this pin is Hi-Z.
- SCL and SDA are connected to the I2C bus inside SVL-03 via a level conversion circuit.
- GPIO pins are controlled via FPGA registers.
- Please do not input signals with voltages exceeding VDDIO to GPIO pins.

6.4. CN11-CN12 Connector for Synchronous Wiring

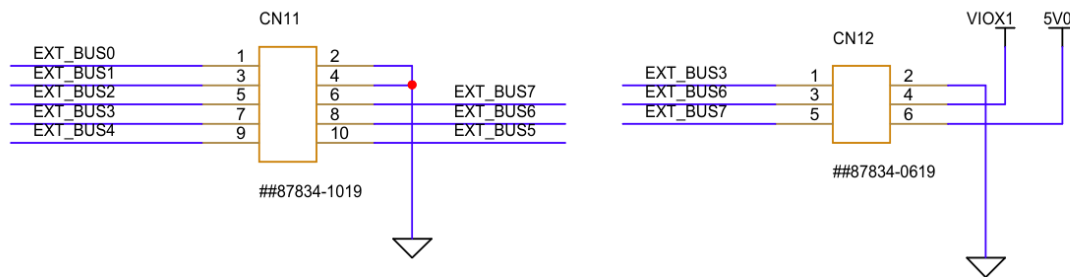
The CN11 and CN12 connectors are used for synchronous wiring between boards, using 2.54 mm pitch IDC connectors. For custom features, these connectors are used to connect multiple boards for capture synchronization and time-stamping functions. They are not used in the standard version.

- Block Diagram



When JP3 on the board is shorted, the EXT_BUS0-3 signal lines are in output status. When JP4 is shorted, the EXT_BUS4-7 signal lines are in output status.

- Pin Assignment



7. Component Details

7.1. SW1: Push Switch

SW1 is used to output a reset signal or retransmit the initial register settings. The function of this switch can be changed via SVMCtl.

When SW1 is assigned to reset output, the RST signal connected to CN4 is asserted (L output) while SW1 is pressed, simultaneously resetting the internal blocks of the FPGA.

When SW1 is assigned to register initialization output, the initial settings stored in the board's SPI-ROM via SVMCtl are retransmitted.

7.2. SW2: DIP Switch

SW2 is an 8bit switch used for setting the various operating modes of SVL-03. The board can be set to the following settings.

- USB mode

No. #	Item	OFF	ON
1	Board number b3	b3 = 0	b3 = 1
2	(Reserved)	Standard operation	
3	(Reserved)	Standard operation	
4	Board number b0	b0 = 0	b0 = 1
5	Board number b1	b1 = 0	b1 = 1
6	Board number b2	b2 = 0	b2 = 1
7	Mode selection (Startup)	7: OFF, 8: OFF -> DisplayPort mode	
		7: ON, 8: OFF -> Updater mode	
8		7: OFF, 8: ON -> USB mode	
		7: ON, 8: ON -> (Reserved)	

– Board numbers b3-b0 are the board numbers recognized by NVFilePlayer.

• DisplayPort mode

No. #	Item	OFF	ON
1	(Reserved)	Standard operation	
2	External synchronization mode (Writing timing data)	Free-run operation	External synchronization enabled
3	(Reserved)	Standard operation	
4	(Reserved)	Standard operation	
5	(Reserved)	Standard operation	
6	(Reserved)	Standard operation	
7	Mode selection (Startup)	7: OFF, 8: OFF -> DisplayPort mode	
8		7: ON, 8: OFF -> Updater mode	
		7: OFF, 8: ON -> USB mode	
		7: ON, 8: ON -> (Reserved)	

- Some additional settings need to be made on SVMctl
- The connection status can be checked on SVMctl.

7.3. LED1-9: Operating Status Indicator

These LEDs display the operating status of the board or FPGA. After a successful startup, the LEDs operate as follows.

LED #	Description
1	Lights up to indicate that the power supply to the target is active. (Red LED)
2	<Reserved>
3	<Reserved>
4	<Reserved>
5	<Reserved>
6	<Reserved>
7	Turns on and off in a cycle of 3 divisions of the V-Sync signal when the internal integrated video sync signal source is being driven.
8	<Reserved>
9	(USB mode) <Reserved> (DisplayPort mode) Turns on and off in a cycle of 3 divisions of the V-Sync signal from DisplayPort receiver.
10	Lights up to indicate that the power supply to the board is active. (Red LED)

- The LEDs labeled as <Reserved> above may be assigned functions in the future. In the current version, their lighting status varies depending on the internal state of the board.

7.4. JP1: VDDIO Selection Jumper

JP1 is used to select the IO power supply (VDDIO) for the target device from the SVL-03. The available options are 1.8V, 2.5V, and 3.3V.

VDDIO is intended to be used as an IO power supply voltage for the target device. Additionally, GPIO0-15, CLK, RST, SCL, and SDA signal lines operate at the VDDIO voltage level.

7.5. JP2: Board Power Setting Jumper

For details, please refer to [CN1: Sub Power Connector](#).

7.6. JP3-JP4: Synchronous Connector Jumper

For details, please refer to [CN11-CN12: Connector for Synchronous Wiring](#).

7.7. Operating Temperature Range

The operating temperature range of the ICs on the SVL-03 is 0-80°C. However, this value does not account for heat generated by the devices themselves. When using the board in a housing, consider attaching a heatsink to the FPGA or using a cooling fan to keep the IC die operating within the 0-80°C range.

For reference, when an LPD25-15B (25x25x15mm) heatsink is attached to the FPGA and used in an open space with natural air cooling, the calculated limit of the upper operating temperature is 35°C in USB mode, 30°C in DisplayPort mode (measured values in our test environment). We have confirmed that the device will operate at temperatures above this limit, but we cannot guarantee that it will function properly.

8. Check Terminal

8.1. TP1-4: GND

These are used as GND (ground) terminals.

8.2. TP5: VDDIO

This is used to verify the voltage of VDDIO.

8.3. TP7-12

These check terminals are for measuring the power supply voltages required for the operation of the SVL-03. Please do not use them to supply power to external devices.

9. Applicable Version

Mode	FX10 Version	FPGA Version
USB mode	0.1.3 or later	1.00 or later
DisplayPort mode	0.3.1 or later	0.30 or later

10. Notes

To ensure proper use of the SVL-03, please follow the precautions below:

1. Turn off the power to this board before connecting or disconnecting the interface board or target.
2. Do not input any external signals when this board is not powered.
3. Use a power supply with sufficient current capacity to ensure stable operation.
4. Turn on the power to the board only after the upstream device has stopped sending signals.
5. When inputting signals from an external device, be careful that the voltage does not exceed the VDDIO voltage of the board
6. If the board is enclosed in a case, consider using a heat sink or cooling fan for proper operation.
7. The contents of this document are subject to change without notice.
8. Reproduction of this document, in whole or in part, without permission is strictly prohibited.
9. If any case any errors or omissions are noticed on this document, please contact us at: E mail: sv-support@net-vision.co.jp

11. Appendix

11.1. CN6: FPGA-JTAG Connector

This JTAG port is used for writing the FPGA bitstream to the SPI-ROM or debugging the FPGA during operation. It is not used for normal use.

*Note: The direction is viewed from the FPGA.

Connector		A3B-14PA-2DSA (71)					
Pin #	Signal	Direction	Description	Pin #	Signal	Direction	Description
1	GND	-		2	VREF	OUT	Reference voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	(Disconnected)
13	GND	-		14	NC	-	(Disconnected)

- Operation is not guaranteed if used.

11.2. CN13: Inspection Connector

This connector is used for inspection before shipment. It is not used for normal use.

11.3. Frame Drops or Image Distortion in USB Mode

- Check that the USB input slew rate has not been exceeded.
- Check that the PC's Type-C port is USB 3.2 Gen 2 compatible.
- The Type-C cable is USB 3.2 Gen 2 compatible.
- If the input slew rate has not been exceeded, open Control Panel -> System and Security -> Power Options and set the power plan to "High Performance". If the PC is a laptop and the option is not available, open System -> Power & Battery and set the power mode to "Optimal Performance".

11.4. When Recognized as an “Unknown USB Device”

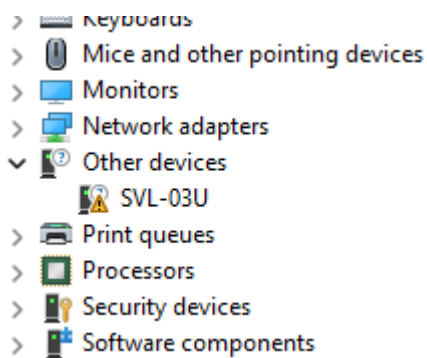
If the board is connected to a PC using a Type-C cable that only supports USB 2.0, it will be recognized as an “Unknown USB Device”. Be sure to use a Type-C cable that supports USB 3.2 Gen 2.

- Device Manager screen when connected via USB2.0.



11.5. When Recognized as “Other Devices”

If the board is recognized as an “Other Devices”, please install the device driver. The device driver is included in the “SVL-03 full package” which can be downloaded from our product support page. Please install the device driver as explained in the manual.



11.6. Connecting to an AMD Graphics Board

In DisplayPort mode, the SVL-03-GEN may not be correctly recognized as a display when connected to an AMD GPU. If it is not recognized correctly, install and launch the AMD Software: Adrenalin Edition application, select the display x that recognizes the SVL-03-GEN, and change the color depth and pixel format to match the EDID written on the board. (Example: 8bpc, RGB 888)

